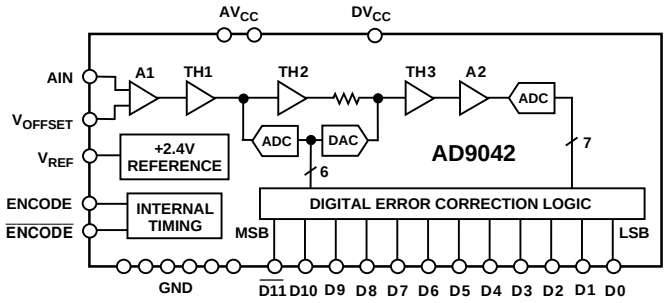
12-Bit, 41 MSPS Monolithic A/D Converter

AD9042

FEATURES
41 MSPS Minimum Sample Rate
80 dB Spurious-Free Dynamic Range
595 mW Power Dissipation
Single +5 V Supply
On-Chip T/H and Reference
Twos Complement Output Format
CMOS-Compatible Output Levels

APPLICATIONS
Cellular/PCS Base Stations
GPS Anti-Jamming Receivers
Communications Receivers
Spectrum Analyzers
Electro-Optics
Medical Imaging
ATE

FUNCTIONAL BLOCK DIAGRAM



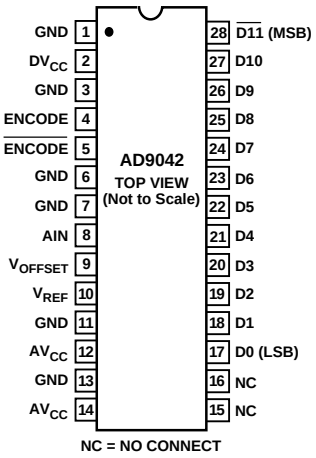
PRODUCT DESCRIPTION

The AD9042 is a high speed, high performance, low power, monolithic 12-bit analog-to-digital converter. All necessary functions, including track-and-hold (T/H) and reference are included on chip to provide a complete conversion solution. The AD9042 runs off of a single +5 V supply and provides CMOS-compatible digital outputs at 41 MSPS.

Designed specifically to address the needs of wideband, multichannel receivers, the AD9042 maintains 80 dB spurious-free dynamic range (SFDR) over a bandwidth of 20 MHz. Noise performance is also exceptional; typical signal-to-noise ratio is 68 dB.

The AD9042 is built on Analog Devices' high speed complementary bipolar process (XFCB) and uses an innovative multipass architecture. Units are packaged in a 28-pin DIP; this custom cofired ceramic package forms a multilayer substrate to which internal bypass capacitors and the 9042 die are attached and a 44-pin TQFP low profile surface mount package. The AD9042 industrial grade is specified from –40°C to +85°C. However, the AD9042 was designed to perform over the full military temperature range (–55°C to +125°C); consult factory for military grade product options.

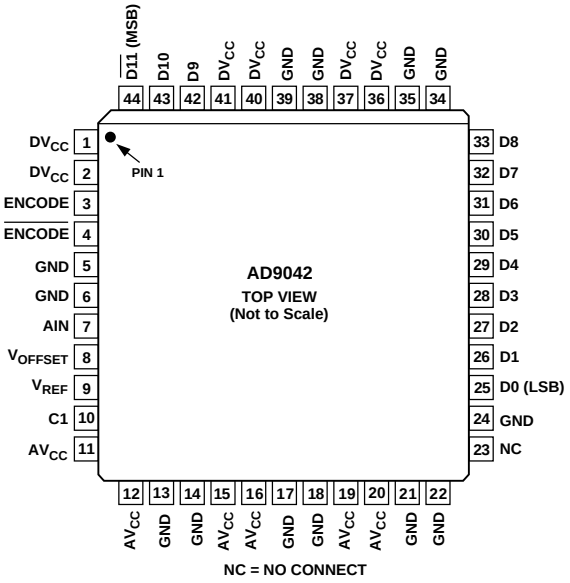
AD9042AD PIN DESIGNATIONS



PRODUCT HIGHLIGHTS

1. Guaranteed sample rate is 41 MSPS.
2. Dynamic performance specified over entire Nyquist band; spurious signals typ. 80 dBc for –1 dBFS input signals.
3. Low power dissipation: 595 mW off a single +5 V supply.
4. Reference and track-and-hold included on chip.
5. Packaged in 28-pin ceramic DIP and 44-pin TQFP.

AD9042AST PIN DESIGNATIONS



REV. A

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AD9042–SPECIFICATIONS

DC SPECIFICATIONS (AV_{CC} = DV_{CC} = +5 V; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = –40°C, T_{MAX} = +85°C)[1]

Parameter	Temp	Test Level	AD9042AST Min	AD9042AST Typ	AD9042AST Max	Test Level	AD9042AD Min	AD9042AD Typ	AD9042AD Max	Units
RESOLUTION				12				12		Bits
DC ACCURACY										
No Missing Codes	Full	VI		Guaranteed		VI		Guaranteed		
Offset Error	Full	VI	–10	±3	+10	VI	–10	±3	+10	mV
Offset Tempco	Full	V		25		V		25		ppm/°C
Gain Error	Full	VI	–6.5	0	+6.5	VI	–6.5	0	+6.5	% FS
Gain Tempco	Full	V		–50		V		–50		ppm/°C
REFERENCE OUT (V_{REF})[2]	+25°C	V		2.4		V		2.4		V
ANALOG INPUT (AIN)										
Input Voltage Range				V_{REF} ±0.500				V_{REF} ±0.500		V
Input Resistance	Full	IV	200	250	300	IV	200	250	300	Ω
Input Capacitance	+25°C	V		5.5		V		7		pF
ENCODE INPUT[3]										
Logic Compatibility[4]				TTL/CMOS				TTL/CMOS		
Logic "1" Voltage	Full	VI	2.0		5.0	VI	2.0		5.0	V
Logic "0" Voltage	Full	VI	0		0.8	VI	0		0.8	V
Logic "1" Current (V_{INH} = 5 V)	Full	VI	450	625	800	VI	450	625	800	µA
Logic "0" Current (V_{INL} = 0 V)	Full	VI	–400	–300	–200	VI	–400	–300	–200	µA
Input Capacitance	+25°C	V		2		V		2.5		pF
DIGITAL OUTPUTS										
Logic Compatibility				CMOS				CMOS		
Logic "1" Voltage (I_{OH} = 10 µA)	+25°C	I	3.5	4.2		I	3.5	4.2		V
	Full	IV	3.5			IV	3.5			V
Logic "0" Voltage (I_{OL} = 10 µA)	+25°C	I		0.75	0.80	I		0.75	0.80	V
	Full	IV			0.85	IV			0.85	V
Output Coding				Twos Complement				Twos Complement		
POWER SUPPLY										
AV_{CC} Supply Voltage	Full	VI		5.0		VI		5.0		V
I (AV_{CC}) Current	Full	V		109		V		109		mA
DV_{CC} Supply Voltage	Full	VI		5.0		VI		5.0		V
I (DV_{CC}) Current	Full	V		10		V		10		mA
I_{CC} (Total) Supply Current	Full	VI		119	147	VI		119	147	mA
Power Dissipation	Full	VI		595	735	VI		595	735	mW
Power Supply Rejection	+25°C	I	–20	±1	+20	I	–20	±1	+20	mV/V
(PSRR)	Full	V		±5		V		±5		mV/V

NOTES
[1]C1 (Pin 10 on AD9042AST only) tied to GND through 0.01 µF capacitor.
[2]V_{REF} is normally tied to V_{OFFSET} through 50 Ω. If V_{REF} is used to provide dc offset to other circuits, it should first be buffered.
[3]ENCODE driven by single-ended source; $\overline{\text{ENCODE}}$ bypassed to ground through 0.01 µF capacitor.
[4]ENCODE may also be driven differentially in conjunction with $\overline{\text{ENCODE}}$; see "Encoding the AD9042" for details.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS (AV_{CC} = DV_{CC} = +5 V; ENCODE & $\overline{\textbf{ENCODE}}$ = 41 MSPS; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = –40°C, T_{MAX} = +85°C)[1]

Parameter (Conditions)	Temp	Test Level	AD9042AST Min	AD9042AST Typ	AD9042AST Max	Test Level	AD9042AD Min	AD9042AD Typ	AD9042AD Max	Units
Maximum Conversion Rate	Full	VI	41			VI	41			MSPS
Minimum Conversion Rate	Full	IV			5	IV			5	MSPS
Aperture Delay (t_A)	+25°C	V		–250		V		–250		ps
Aperture Uncertainty (Jitter)	+25°C	V		0.7		V		0.7		ps rms
ENCODE Pulse Width High	+25°C	IV	10			IV	10			ns
ENCODE Pulse Width Low	+25°C	IV	10			IV	10			ns
Output Delay (t_{OD})	Full	IV	5	9	14	IV	5	9	14	ns

NOTE
[1]C1 (Pin 10 on AD9042AST only) tied to GND through 0.01 µF capacitor.

AC SPECIFICATIONS[1] (AV_{CC} = DV_{CC} = +5 V; ENCODE & $\overline{\text{ENCODE}}$ = 41 MSPS; V_{REF} tied to V_{OFFSET} through 50 Ω; T_{MIN} = –40°C, T_{MAX} = +85°C)[2]

Parameter (Conditions)	Temp	Test Level	AD9042AST Min	AD9042AST Typ	AD9042AST Max	Test Level	AD9042AD Min	AD9042AD Typ	AD9042AD Max	Units
SNR[3]										
Analog Input 1.2 MHz	+25°C	V		68		I	65	68		dB
@ –1 dBFS	Full	V		67.5		V		67.5		dB
9.6 MHz	+25°C	V		67.5		I	64.5	67.5		dB
	Full	V		67		V		67		dB
19.5 MHz	+25°C	I	64	67		I	64	67		dB
	Full	V		66.5		V		66.5		dB
SINAD[4]										
Analog Input 1.2 MHz	+25°C	V		67.5		I	64	67.5		dB
@ –1 dBFS	Full	V		67		V		67		dB
9.6 MHz	+25°C	V		67.5		I	64	67.5		dB
	Full	V		67		V		67		dB
19.5 MHz	+25°C	I	64	67		I	64	67		dB
	Full	V		66.5		V		66.5		dB
Worst Spur[5]										
Analog Input 1.2 MHz	+25°C	V		80		I	74	80		dBc
@ –1 dBFS	Full	V		78		V		78		dBc
9.6 MHz	+25°C	V		80		I	74	80		dBc
	Full	V		78		V		78		dBc
19.5 MHz	+25°C	I	73	80		I	73	80		dBc
	Full	V		78		V		78		dBc
Small Signal SFDR (w/Dither)[6]										
Analog Input @1.2 MHz	Full	V		90		V		90		dBFS
9.6 MHz	Full	V		90		V		90		dBFS
19.5 MHz	Full	V		90		V		90		dBFS
Two-Tone IMD Rejection[7]										
F1, F2 @ –7 dBFS	Full	V		80		V		80		dBc
Two-Tone SFDR (w/Dither)[8]	Full	V		90		V		90		dBFS
Thermal Noise	+25°C	V		0.33		V		0.33		LSB rms
Differential Nonlinearity	+25°C	I	–1.0	±0.3	+1.0	I	–1.0	±0.3	+1.0	LSB
(ENCODE = 20 MSPS)	Full	V		±0.4		VI	–1.0		+1.25	LSB
Integral Nonlinearity (ENCODE = 20 MSPS)	Full	V		±0.75		V		±0.75		LSB
Analog Input Bandwidth	+25°C	V		100		V		100		MHz
Transient Response	+25°C	V		10		V		10		ns
Overvoltage Recovery Time	+25°C	V		25		V		25		ns

NOTES

[1]All ac specifications tested by driving ENCODE and $\overline{\text{ENCODE}}$ differentially; see "ENCODING the AD9042" for details.

[2]C1 (Pin 10 on AD9042AST only) tied to GND through 0.01 µF capacitor.

[3]Analog input signal power at –1 dBFS; signal-to-noise ratio (SNR) is the ratio of signal level to total noise (first five harmonics removed).

[4]Analog input signal power at –1 dBFS; signal-to-noise and distortion (SINAD) is the ratio of signal level to total noise + harmonics.

[5]Analog input signal power at –1 dBFS; worst spur is the ratio of the signal level to worst spur, usually limited by harmonics.

[6]Analog input signal power swept from –20 dBFS to –95 dBFS; dither power = –32.5 dBm; dither circuit used on input signal (see "Overcoming Static Nonlinearities with Dither"); SFDR is ratio of converter full scale to worst spur.

[7]Tones at –7 dBFS (F1 = 15.3 MHz, F2 = 19.5 MHz); two tone intermodulation distortion (IMD) rejection is ratio of either tone to worst third order intermod product.

[8]Both input tones swept from –20 to –95 dBFS; Dither power = –32.5 dBm; dither circuit used on input signal (see "Overcoming Static Nonlinearities with Dither); two tone spurious-free dynamic range (SFDR) is the ratio of converter full scale to worst spur.

Specifications subject to change without notice.

WAFER TEST LIMITS[1] (AV_{CC} = DV_{CC} = +5 V; ENCODE = 10.3 MSPS unless otherwise noted)

Parameter	Temp	AD9042CHIPS Min	Max	Units
POWER SUPPLY				
I_{CC} Supply Current	+25°C	90	147	mA
ENCODE Input				
Logic "1" Current	+25°C	450	800	µA
Logic "0" Current	+25°C	–400	–200	µA
DC ACCURACY				
Offset Error	+25°C	–8	8	mV
Gain Error	+25°C	–6	6	% FS
No Missing Codes	+25°C	Guaranteed		
Differential Nonlinearity @ 5.3 MSPS	+25°C	–0.995		LSB

NOTES
[1]Electrical test is performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice.
[2]Die substrate is connected to 0 V.

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Min	Max	Units
ELECTRICAL			
AV_{CC} Voltage	0	7	V
DV_{CC} Voltage	0	7	V
Analog Input Voltage	0.5	4.5	V
Analog Input Current		20	mA
Digital Input Voltage (ENCODE)	0	AV_{CC}	V
ENCODE, $\overline{\text{ENCODE}}$ Differential Voltage		4	V
Digital Output Current	–40	40	mA
ENVIRONMENTAL[2]			
Operating Temperature Range (Ambient)	–40	+85	°C
Maximum Junction Temperature			
AD9042AD		+175	°C
AD9042AST		+150	°C
Lead Temperature (Soldering, 10 sec)		+300	°C
Storage Temperature Range (Ambient)	–65	+150	°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances for "D" package (custom ceramic 28-pin DIP): θ_{JC} = 14°C/W; θ_{JA} = 34°C/W. For "ST" package (44-pin TQFP) ; θ_{JA} = 55°C/W.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures. AC testing done on sample basis.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% production tested at +25°C; sample tested at temperature extremes.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9042AST	–40°C to +85°C (Ambient)	44-Pin TQFP (Thin Quad Plastic Flatpack)	ST-44
AD9042AD	–40°C to +85°C (Ambient)	28-Pin 600 Mil Hermetic Ceramic DIP (DH-28)	DH-28
AD9042CHIPS	–40°C to +85°C (Ambient)	Unpackaged Die	
AD9042ST/PCB		Evaluation Board with AD9042AST	
AD9042D/PCB		Evaluation Board with AD9042AD	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9042 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD9042AST PIN DESCRIPTIONS

Pin No.	Name	Function
1, 2	DV_{CC}	+5 V Power Supply (Digital). Powers output stage only.
3	ENCODE	Encode input. Data conversion initiated on rising edge.
4	$\overline{\text{ENCODE}}$	Complement of ENCODE. Drive differentially with ENCODE or bypass to Ground for single-ended clock mode.
5, 6	GND	Ground.
7	AIN	Analog Input.
8	V_{OFFSET}	Voltage Offset Input. Sets mid-point of analog input range. Normally tied to V_{REF} through 50 Ω resistor.
9	V_{REF}	Internal Voltage Reference. Nominally +2.4 V; normally tied to V_{OFFSET} through 50 Ω resistor. Bypass to Ground with 0.1 µF + 0.01 µF microwave chip cap.
10	C1	Internal Bias Point. Bypass to ground with 0.01 µF cap.
11, 12	AV_{CC}	+5 V Power Supply (Analog).
13, 14	GND	Ground.
15, 16	AV_{CC}	+5 V Power Supply (Analog).
17, 18	GND	Ground.
19, 20	AV_{CC}	+5 V Power Supply (Analog).
21	GND	Ground.
22	GND	Ground.
23	NC	No Connects.
24	GND	Ground.
25	D0 (LSB)	Digital Output Bit (Least Significant Bit)
26–33	D1–D8	Digital Output Bits
34, 35	GND	Ground.
36, 37	DV_{CC}	+5 V Power Supply (Digital). Powers output stage only.
38, 39	GND	Ground.
40, 41	DV_{CC}	+5 V Power Supply (Digital). Powers Output Stage only.
42, 43	D9–D10	Digital Output Bits.
44	$\overline{\text{D11}}$ (MSB)[1]	Digital Output Bit (Most Significant Bit).

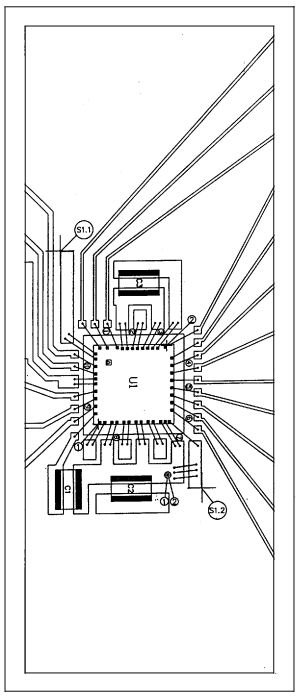
NOTE
[1]Output coded as twos complement.

AD9042AD PIN DESCRIPTIONS

Pin No.	Name	Function
1	GND	Ground.
2	DV_{CC}	+5 V Power Supply (Digital). Powers output stage only.
3	GND	Ground.
4	ENCODE	Encode input. Data conversion initiated on rising edge.
5	$\overline{\text{ENCODE}}$	Complement of ENCODE. Drive differentially with ENCODE or bypass to Ground for single-ended clock mode.
6, 7	GND	Ground.
8	AIN	Analog Input.
9	V_{OFFSET}	Voltage Offset Input. Sets mid-point of analog input range. Normally tied to V_{REF} through 50 Ω resistor.
10	V_{REF}	Internal Voltage Reference. Nominally +2.4 V; normally tied to V_{OFFSET} through 50 Ω resistor. Bypass to Ground with 0.1 µF cap.
11	GND	Ground.
12	AV_{CC}	+5 V Power Supply (Analog).
13	GND	Ground.
14	AV_{CC}	+5 V Power Supply (Analog).
15, 16	NC	No Connects.
17	D0 (LSB)	Digital Output Bit. (Least Significant Bit).
18–27	D1–D10	Digital Output Bits.
28	$\overline{\text{D11}}$ (MSB)[1]	Digital Output Bit (Most Significant Bit).

NOTE
[1]Output coded as twos complement.

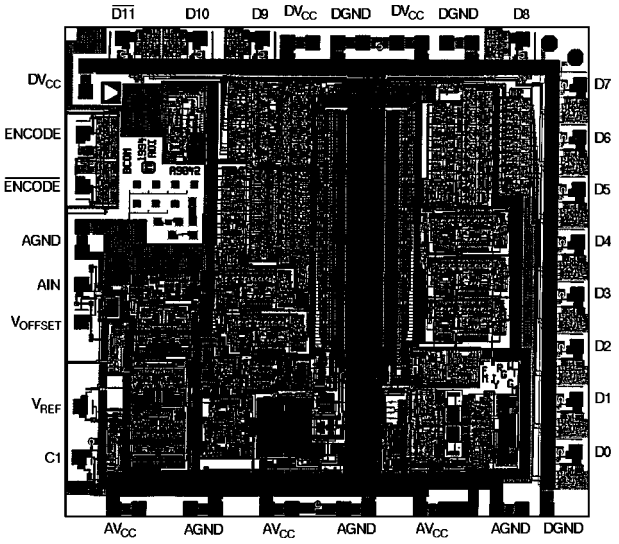
AD9042 CUSTOM 28-PIN DIP PACKAGE



DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions	$155 \times 168 \times 21$ (± 1) mils
Pad Dimensions	4×4 mils
Metalization	Aluminum
Backing	None
Substrate Potential	GND
Transistor Count	2,605
Passivation	Oxynitride
Die Attach	Silver Filled
Bond Wire	Gold

DIE LAYOUT W/PAD LABELS



DEFINITION OF SPECIFICATIONS

Analog Bandwidth
The analog input frequency at which the spectral power of the fundamental frequency (as determined by the FFT analysis) is reduced by 3 dB.

Aperture Delay
The delay between the 50% point of the rising edge of the ENCODE command and the instant at which the analog input is sampled.

Aperture Uncertainty (Jitter)
The sample-to-sample variation in aperture delay.

Differential Nonlinearity
The deviation of any code from an ideal 1 LSB step.

Encode Pulse Width/Duty Cycle
Pulse width high is the minimum amount of time that the ENCODE pulse should be left in logic "1" state to achieve rated performance; pulse width low is the minimum time ENCODE pulse should be left in low state. At a given clock rate, these specs define an acceptable Encode duty cycle.

Harmonic Distortion
The ratio of the rms signal amplitude to the rms value of the worst harmonic component, reported in dBc.

Integral Nonlinearity
The deviation of the transfer function from a reference line measured in fractions of 1 LSB using a "best straight line" determined by a least square curve fit.

Minimum Conversion Rate
The encode rate at which the SNR of the lowest analog signal frequency drops by no more than 3 dB below the guaranteed limit.

Maximum Conversion Rate
The encode rate at which parametric testing is performed.

Output Propagation Delay
The delay between the 50% point of the rising edge of ENCODE command and the time when all output data bits are within valid logic levels.

Overvoltage Recovery Time
The amount of time required for the converter to recover to 0.02% accuracy after an analog input signal 150% of full scale is reduced to midscale.

Power Supply Rejection Ratio
The ratio of a change in input offset voltage to a change in power supply voltage.

Signal-to-Noise-and-Distortion (SINAD)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, including harmonics but excluding dc.

Signal-to-Noise Ratio (without Harmonics)
The ratio of the rms signal amplitude (set at 1 dB below full scale) to the rms value of the sum of all other spectral components, excluding the first five harmonics and dc.

Spurious-Free Dynamic Range
The ratio of the rms signal amplitude to the rms value of the peak spurious spectral component. The peak spurious component may or may not be a harmonic. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

Transient Response
The time required for the converter to achieve 0.02% accuracy when a one-half full-scale step function is applied to the analog input.

Two-Tone Intermodulation Distortion Rejection
The ratio of the rms value of either input tone to the rms value of the worst third order intermodulation product; reported in dBc.

Two-Tone SFDR
The ratio of the rms value of either input tone to the rms value of the peak spurious component. The peak spurious component may or may not be an IMD product. May be reported in dBc (i.e., degrades as signal levels is lowered), or in dBFS (always related back to converter full scale).

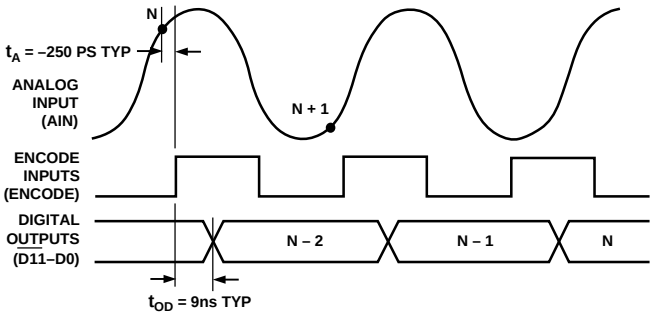


Figure 1. Timing Diagram

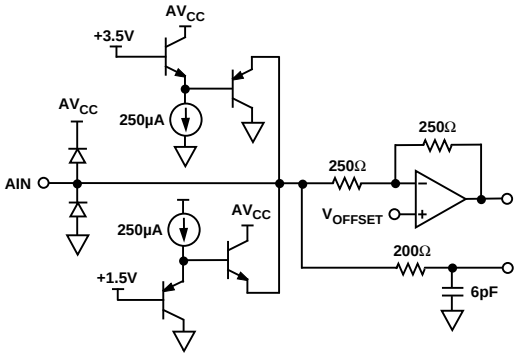


Figure 2. Analog Input Stage

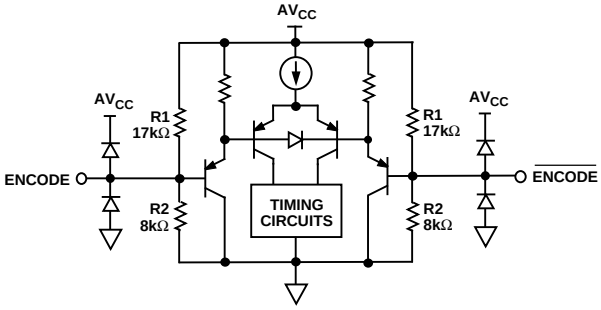


Figure 3. Encode Inputs

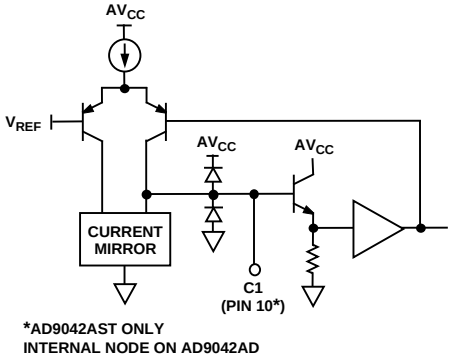


Figure 4. Compensation Pin, C1

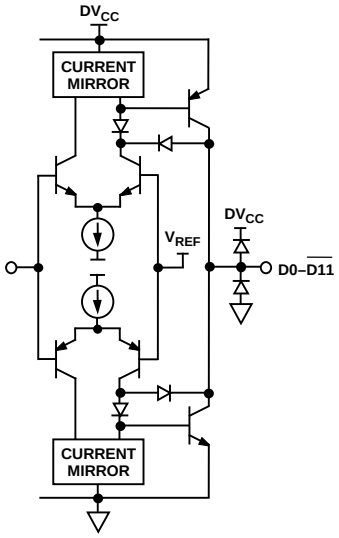


Figure 5. Digital Output Stage

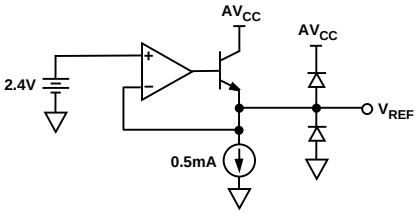
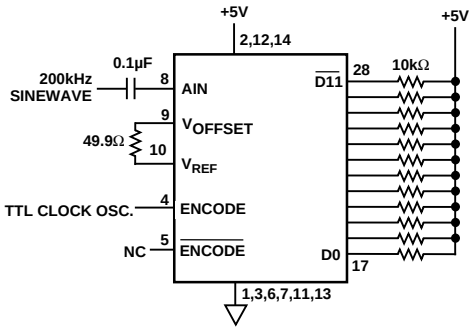


Figure 6. 2.4 V Reference



NOTE: ALL +5V SUPPLY PINS & V_{REF} PIN BYPASSED TO GND WITH A 0.1µF CAPACITOR. PINS 15,16 ARE NOT CONNECTED.

Figure 7. AD9042AD Burn-In Diagram

AD9042–Typical Performance Characteristics

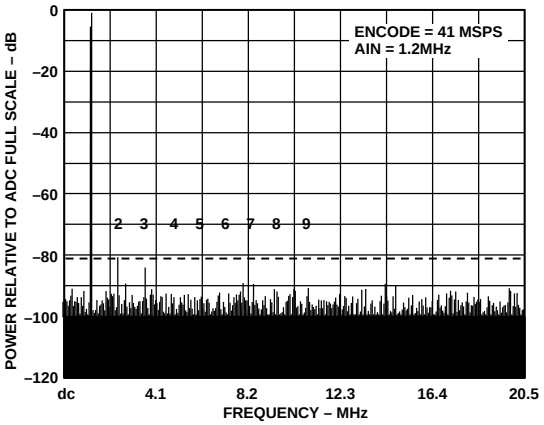


Figure 8. Single Tone at 1.2 MHz

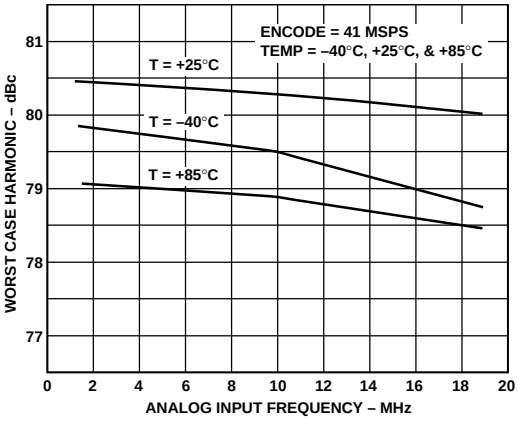


Figure 11. Harmonics vs. AIN

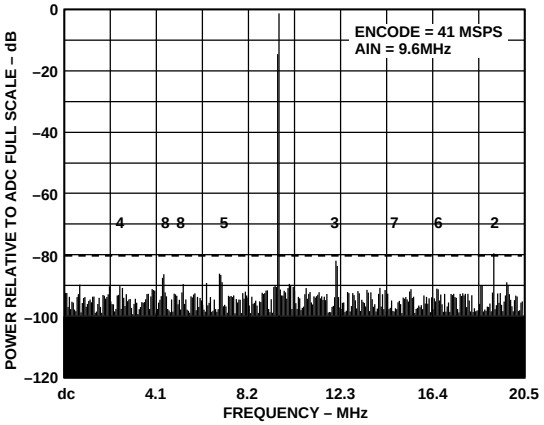


Figure 9. Single Tone at 9.6 MHz

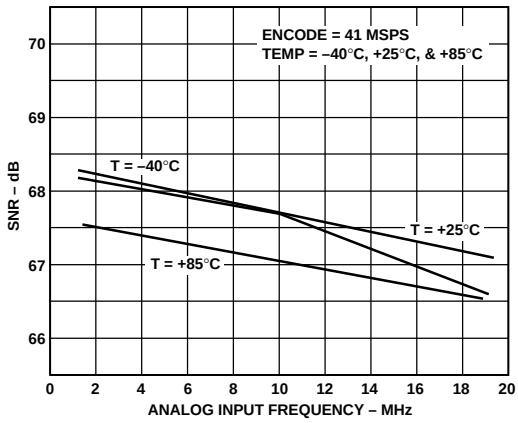


Figure 12. Noise vs. AIN

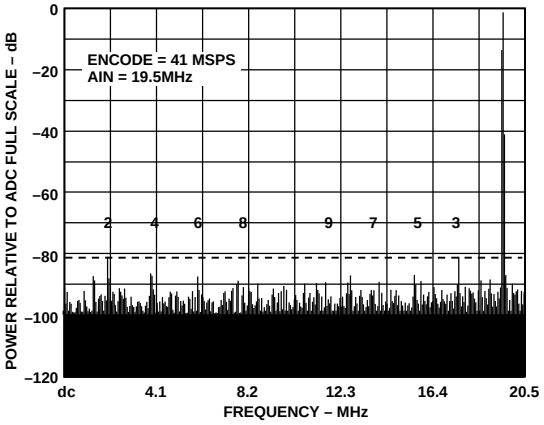


Figure 10. Single Tone at 19.5 MHz

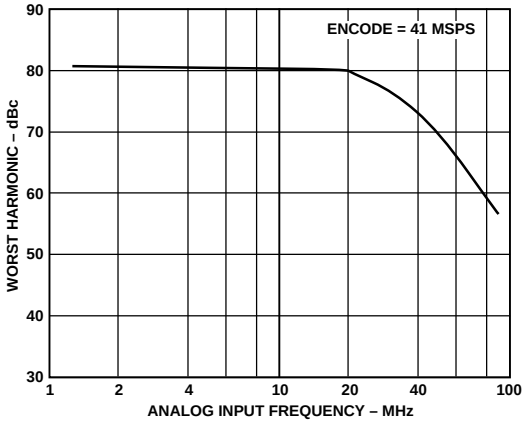


Figure 13. Harmonics vs. AIN

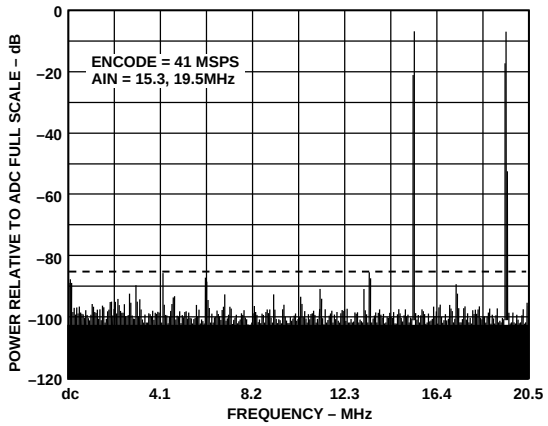


Figure 14. Two Tones at 15.3 MHz & 19.5 MHz

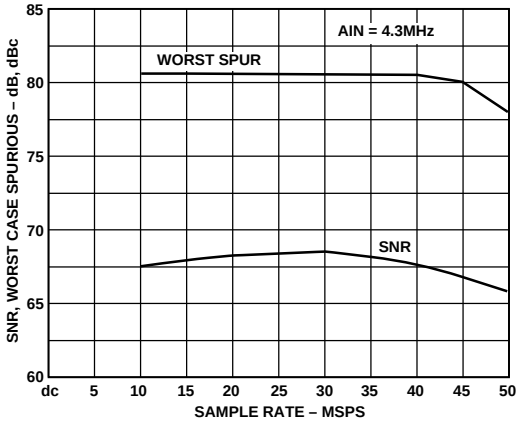


Figure 17. SNR, Worst Harmonic vs. Encode

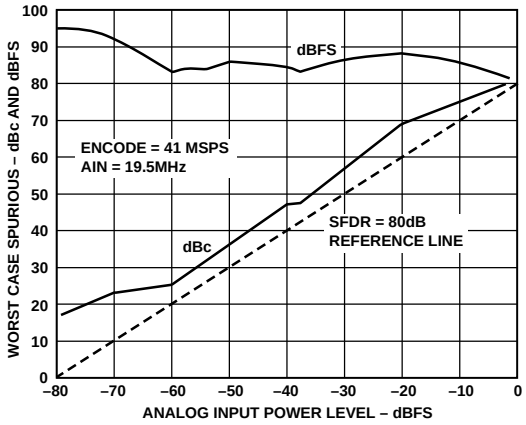


Figure 15. AD9042AD Single Tone SFDR

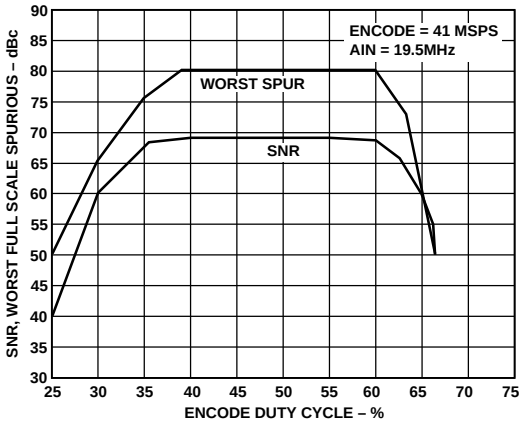


Figure 18. SNR, Worst Spurious vs. Duty Cycle

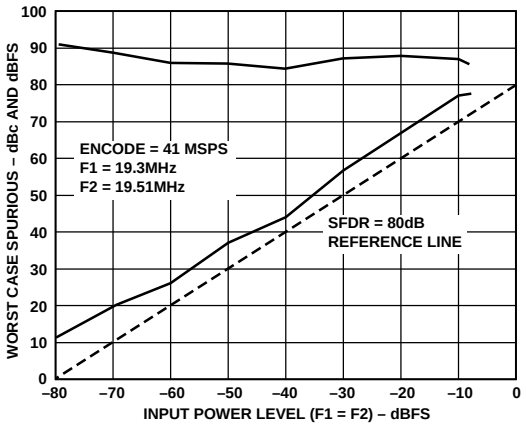


Figure 16. AD9042AD Two Tone SFDR

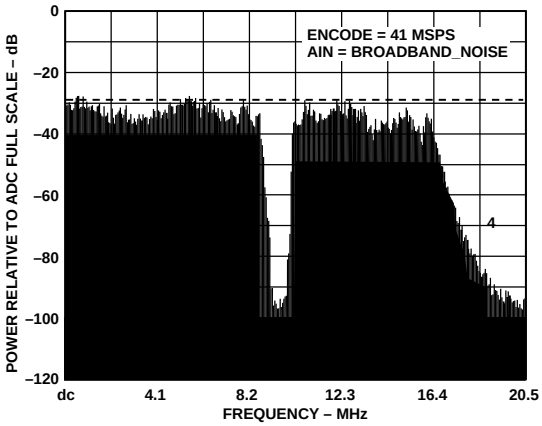


Figure 19. NPR Output Spectrum

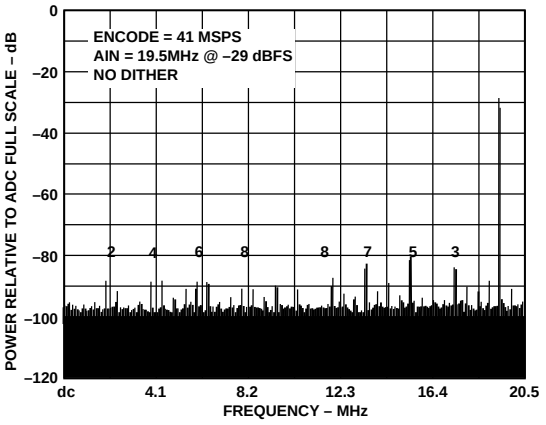


Figure 20. 4K FFT without Dither

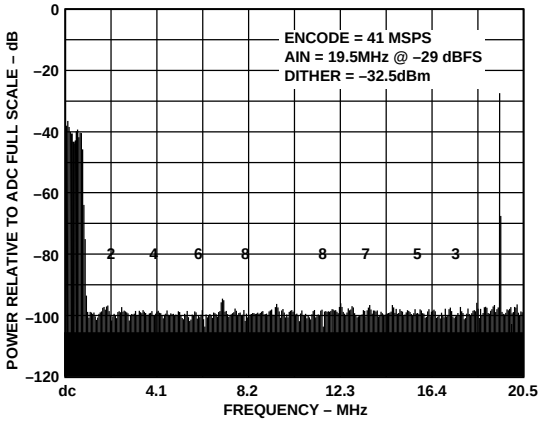


Figure 23. 4K FFT with Dither

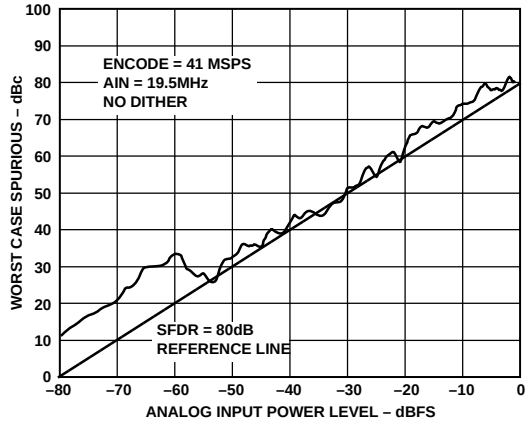


Figure 21. SFDR without Dither

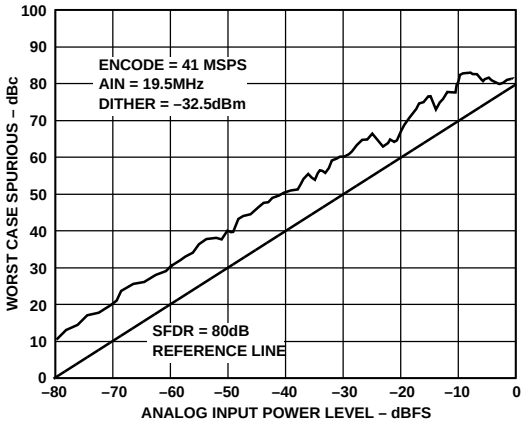


Figure 24. SFDR with Dither

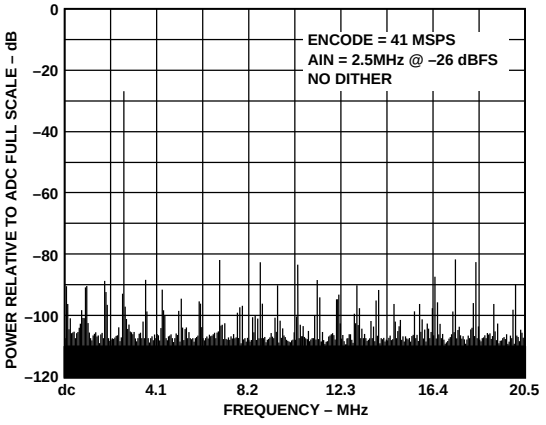


Figure 22. 128K FFT without Dither

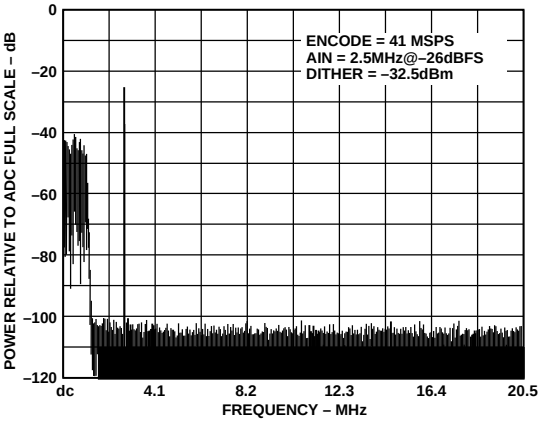


Figure 25. 128K FFT with Dither

THEORY OF OPERATION

The AD9042 analog-to-digital converter (ADC) employs a two-stage subrange architecture. This design approach ensures 12-bit accuracy, without the need for laser trim, at low power.

As shown in the functional block diagram, the 1 V p-p single-ended analog input, centered at 2.4 V, drives a single-in to differential-out amplifier, A1. The output of A1 drives the first track-and-hold, TH1. The high state of the ENCODE pulse places TH1 in hold mode. The held value of TH1 is applied to the input of the 6-bit coarse ADC. The digital output of the coarse ADC drives a 6-bit DAC; the DAC is 12 bits accurate. The output of the 6-bit DAC is subtracted from the delayed analog signal at the input to TH3 to generate a residue signal. TH2 is used as an analog pipeline to null out the digital delay of the coarse ADC.

The residue signal is passed to TH3 on a subsequent clock cycle where the signal is amplified by the residue amplifier, A2, and converted to a digital word by the 7-bit residue ADC. One bit of overlap is used to accommodate any linearity errors in the coarse ADC.

The 6-bit coarse ADC word and 7-bit residue word are added together and corrected in the digital error correction logic to generate the output word. The result is a 12-bit parallel digital word which is CMOS-compatible, coded as twos complement.

APPLYING THE AD9042

Encoding the AD9042

The AD9042 is designed to interface with TTL and CMOS logic families. The source used to drive the ENCODE pin(s) must be clean and free from jitter. Sources with excessive jitter will limit SNR (ref. Equation 1 under "Noise Floor and SNR").

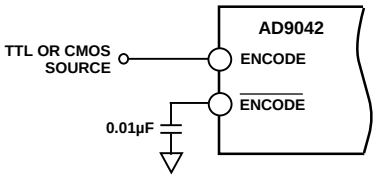


Figure 26. Single-Ended TTL/CMOS Encode

The AD9042 encode inputs are connected to a differential input stage (see Figure 3 under EQUIVALENT CIRCUITS). With no input connected to either the ENCODE or input, the voltage dividers bias the inputs to 1.6 volts. For TTL or CMOS usage, the encode source should be connected to ENCODE. $\overline{\text{ENCODE}}$ should be decoupled using a low inductance or microwave chip capacitor to ground. Devices such as AVX 05085C103MA15, a 0.01 µF capacitor, work well.

If a logic threshold other than the nominal 1.6 V is required, the following equations show how to use an external resistor, R_X, to raise or lower the trip point (see Figure 3; R1 = 17k, R2 = 8k).

$$V_1 = \frac{5R_2R_X}{R_1R_2 + R_1R_X + R_2R_X}$$ to lower logic threshold.

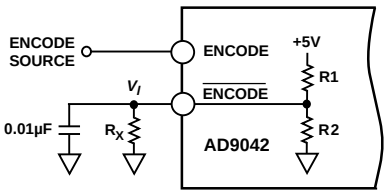


Figure 27. Lower Logic Threshold for Encode

$$V_1 = \frac{5R_2}{R_2 + \frac{R_1R_X}{R_1 + R_X}}$$ to raise logic threshold.

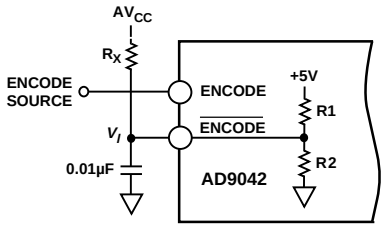


Figure 28. Raise Logic Threshold for Encode

While the single-ended encode will work well for many applications, driving the encode differentially will provide increased performance. Depending on circuit layout and system noise, a 1 dB to 3 dB improvement in SNR can be realized. It is not recommended that differential TTL logic be used however, because most TTL families that support complementary outputs are not delay or slew rate matched. Instead, it is recommended that the encode signal be ac-coupled into the ENCODE and $\overline{\text{ENCODE}}$ pins.

The simplest option is shown below. The low jitter TTL signal is coupled with a limiting resistor, typically 100 ohms, to the primary side of an RF transformer (these transformers are inexpensive and readily available; part# in Figure 29 is from Mini-Circuits). The secondary side is connected to the ENCODE and $\overline{\text{ENCODE}}$ pins of the converter. Since both encode inputs are self biased, no additional components are required.

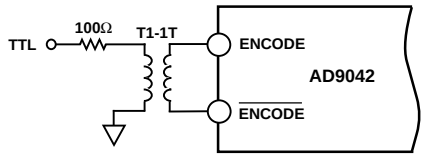


Figure 29. TTL Source – Differential Encode

If no TTL source is available, a clean sine wave may be substituted. In the case of the sine source, the matching network is shown below. Since the matching transformer specified is a 1:1 impedance ratio, R, the load resistor should be selected to match the source impedance. The input impedance of the AD9042 is negligible in most cases.

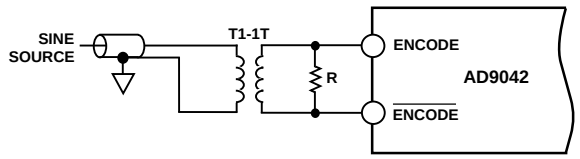


Figure 30. Sine Source – Differential Encode

If a low jitter ECL clock is available, another option is to ac-couple a differential ECL signal to the encode input pins as shown below. The capacitors shown here should be chip capacitors but do not need to be of the low inductance variety.

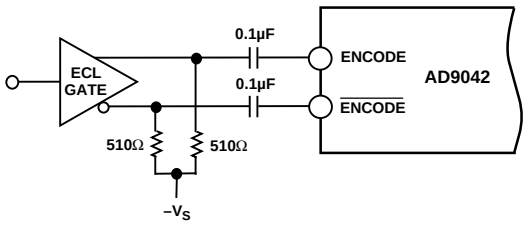


Figure 31. Differential ECL for Encode

As a final alternative, the ECL gate may be replaced by an ECL comparator. The input to the comparator could then be a logic signal or a sine signal.

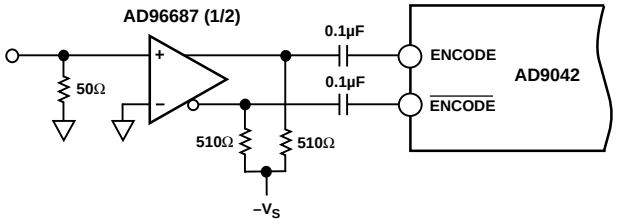


Figure 32. ECL Comparator for Encode

Care should be taken not to overdrive the encode input pin when ac coupled. Although the input circuitry is electrically protected from over or under voltage conditions, improper circuit operations may result from overdriving the encode input pins.

Driving the Analog Input

Because the AD9042 operates off of a single +5 V supply, the analog input range is offset from ground by 2.4 volts. The analog input, AIN, is an operational amplifier configured in an inverting mode (ref. Equivalent Circuits: Analog Input Stage). V_{OFFSET} is the noninverting input which is normally tied through a 50 ohm resistor to V_{REF} (ref. Equivalent Circuits: 2.4 V Reference). Since the operational amplifier forces its inputs to the same voltage, the inverting input is also at 2.4 volts. Therefore, the analog input has a Thevenin equivalent of 250 ohms in series with a 2.4 volt source. It is strongly recommended that the AD9042's internal voltage reference be used for the amplifier offset; this reference is designed to track internal circuit shifts over temperature.

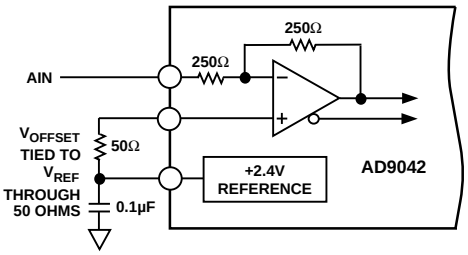


Figure 33. Analog Input Offset by +2.4 V Reference

Although the AD9042 may be used in many applications, it was specifically designed for communications systems which must digitize wide signal bandwidths. As such, the analog input was designed to be ac-coupled. Since most communications products do not down-convert to dc, this should not pose a problem. One example of a typical analog input circuit is shown below. In this application, the analog input is coupled with a high quality chip capacitor, the value of which can be chosen to provide a low frequency cutoff that is consistent with the signal being sampled; in most cases, a 0.1 µF chip capacitor will work well.

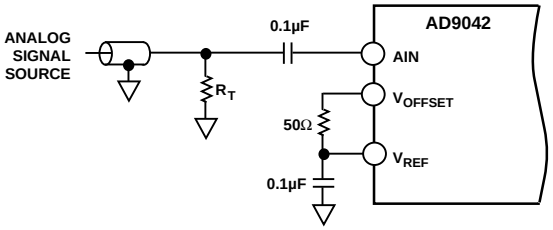


Figure 34. AC-Coupled Analog Input Signal

Another option for ac-coupling is a transformer. The impedance ratio and frequency characteristics of the transformer are determined by examining the characteristics of the input signal source (transformer primary connection), and the AD9042 input characteristics (transformer secondary connection). "R_T" should be chosen to satisfy termination requirements of the source, given the transformer turns ratio. A blocking capacitor is required to prevent AD9042 dc bias currents from flowing through the transformer.

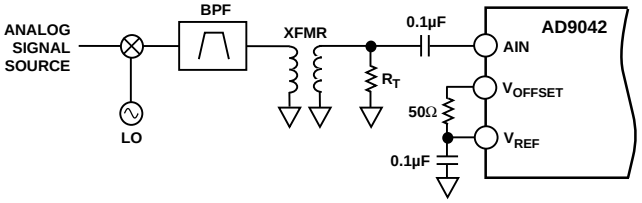


Figure 35. Transformer-Coupled Analog Input Signal

When calculating the proper termination resistor, note that the external load resistor is in parallel with the AD9042 analog input resistance, 250 ohms. The external resistor value can be calculated from the following equation:

$$R_T = \frac{1}{\frac{1}{Z} - \frac{1}{250}}$$

where Z is desired impedance.

A dc-coupled input configuration (shown below) is limited by the drive amplifier performance. The AD9042's on-chip reference is buffered using the OP279 dual, rail-to-rail operational amplifier. The resulting voltage is combined with the analog source using an AD9631. Pending improvements in drive amplifiers, this dc-coupled approach is limited to ~75 dB–80 dB of dynamic performance depending on which drive amplifier is used. The AD9631 and OP279 run off ±5 V.

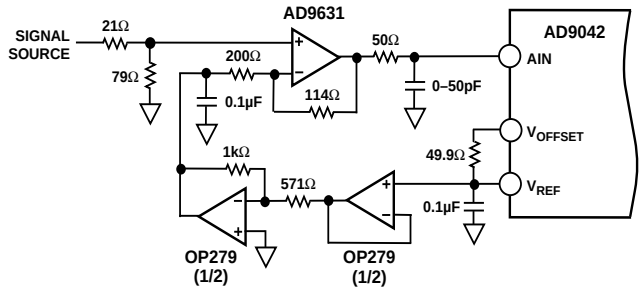


Figure 36. DC-Coupled Analog Input Circuit

Power Supplies

Care should be taken when selecting a power source. Linear supplies are strongly recommended as switching supplies tend to have radiated components that may be "received" by the AD9042. Each of the power supply pins should be decoupled as closely to the package as possible using 0.1 µF chip capacitors.

The AD9042 has separate digital and analog +5 V pins. The analog supplies and the denoted AV_{CC} digital supply pins are denoted DV_{CC}. Although analog and digital supplies may be tied together, best performance is achieved when the supplies are separate. This is because the fast digital output swings can couple switching noise back into the analog supplies. Note that AV_{CC} must be held within 5% of 5 volts, however the DV_{CC} supply may be varied according to output digital logic family (i.e., DV_{CC} should be connected to the supply for the digital circuitry).

Output Loading

Care must be taken when designing the data receivers for the AD9042. It is recommended that the digital outputs drive a series resistor of 499 ohms followed by a CMOS gate like the 74AC574. To minimize capacitive loading, there should only be one gate on each output pin. An example of this is shown in the evaluation board schematics shown in Figures 37 and 38. The digital outputs of the AD9042 have a unique constant slew rate output stage. The output slew rate is about 1 V/ns independent of output loading. A typical CMOS gate combined with PCB trace and through hole will have a load of approximately 10 pF. Therefore as each bit switches, 10 mA

$\left(10\,pF \times \frac{1V}{1\,ns}\right)$ of dynamic current per bit will flow in or out of

the device. A full- scale transition can cause up to 120 mA (12 bits × 10 mA/bit) of current to flow through the digital output stage. The series resistor will minimize the output currents that can flow in the output stage. These switching currents are confined between ground and the DV_{CC} pin. Standard TTL gates should be avoided since they can appreciably add to the dynamic switching currents of the AD9042.

Layout Information

The schematic of the evaluation boards (Figures 37 and 38) represents a typical implementation of the AD9042. The pinout of the AD9042 facilitates ease of use and the implementation of high frequency/high resolution design practices. All of the digital outputs are on one side of the packages while the other sides contain all of the inputs. It is highly recommended that high quality ceramic chip capacitors be used to decouple each supply pin to ground directly at the device. Depending on the configuration used for the encode and analog inputs, one or more capacitors are required on those input pins. The capacitors used on the $\overline{\text{ENCODE}}$ and V_{REF} pins must be a low inductance chip capacitor as referenced previously in the data sheet.

Although a multilayer board is recommended, it is not required to achieve good results. As shown in the DIP evaluation board layout (Figures 39–42), the top layer forms a near solid ground plane while the under side is used for routing signal. No vias or jumpers are required to route signals in and out of the AD9042AD. Each supply is decoupled to ground directly at the device.

Care should be taken when placing the digital output runs. Because the digital outputs have such a high slew rate, the capacitive loading on the digital outputs should be minimized. Circuit traces for the digital outputs should be kept short and connect directly to the receiving gate (broken only by the insertion of the series resistor). Logic fanout for each bit should be one CMOS gate.

Evaluation Boards

The evaluation board for the AD9042 is very straight forward consisting of power, signal inputs and digital outputs. The evaluation board includes an onboard clock oscillator for the encode; all the user must supply is power and an analog signal.

Power to the analog supply pins is connected via banana jacks. The analog supply powers the crystal oscillator and the AV_{CC} pins of the AD9042. The DV_{CC} power is supplied via J3, the digital interface. This digital supply connection also powers the digital gates on the PCB. By maintaining separate analog and digital power supplies, degradation in SNR and SFDR is kept to a minimum. Total power requirement for either PCB is approximately 140 mA. This configuration allows for easy evaluation of different logic families (i.e., connection to a 3.3 volt logic board).

The analog input is connected via J2 and is capacitively coupled to the AD9042 (see "Driving the Analog Input"). The onboard termination resistor is 60.4 Ω. This resistor in parallel with AD9042's input resistance (250 Ω) provides a 50 Ω load to the analog source. If a different input impedance is required, replace R1 by using the following equation

$$R_1 = \frac{1}{\frac{1}{Z} - \frac{1}{250}}$$ where *Z* is desired input impedance.

The analog input range of PCB is ±0.5 volts (i.e., signal ac-coupled to AD9042).

The encode signal is generated using the onboard crystal oscillator, U1. The oscillator is socketed and may be replaced by an external encode source via J1. If an external source is used, it should be a high quality TTL source. A transformer converts the single-ended TTL signal to a differential clock (see "Encoding the AD9042"). Since the encode is coupled with a

transformer, a sine wave could have been used; however, note that U5 requires TTL levels to function properly.

AD9042 output data is latched using 74ACT574 (U3, U4) latches following 499 ohm series resistors. The resistors limit the current that would otherwise flow due to the digital output slew rate. The resistor value was chosen to represent a time constant of ~25% of the data rate at 40 MHz. This reduces slew rate while not appreciably distorting the data waveform. Data is latched in a pipeline configuration; a rising edge generates the new AD9042 data sample, latches the previous data at the converter output, and strobes the external data register over J3. Power and ground must be applied to J3 to power the digital logic section of the evaluation board.

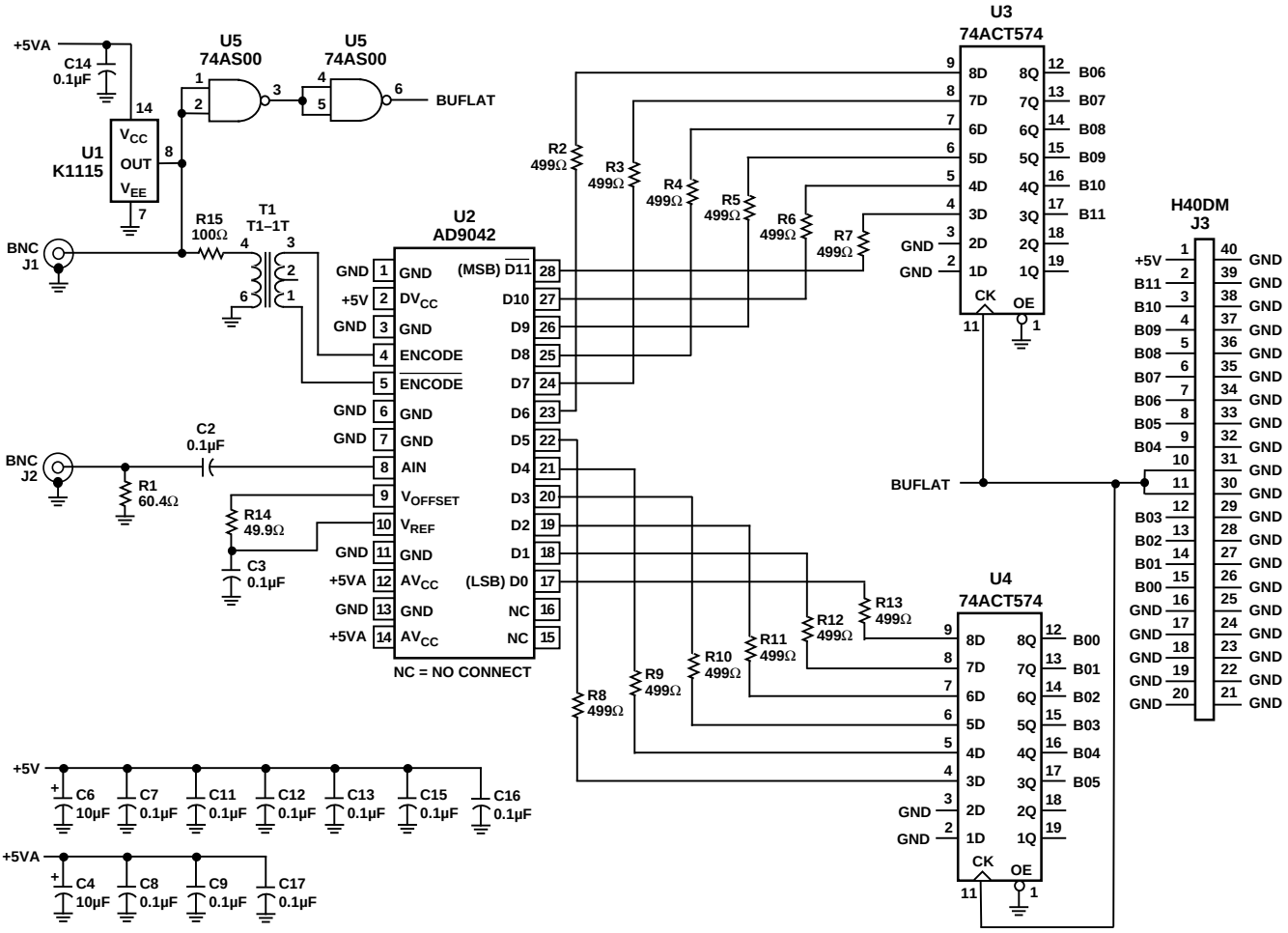


Figure 37. AD9042D/PCB Schematic

Table I. AD9042D/PCB Bill of Material

Item	Quantity	Reference	Description
1	2	+5VA, GND	Banana Jack
2	10	C2–C3, C7–C9, C11–C17	Ceramic Chip Capacitor 0805, 0.1 µF
3	2	C4, C6	Tantalum Chip Capacitor 10 µF
4	1	J3	40-Pin Double Row Male Header
5	2	J1, J2	BNC Coaxial PCB Connector
6	1	R1	Surface Mount Resistor 1206, 60.4 ohms
7	12	R2–R13	Surface Mount Resistor 1206, 499 ohms
8	1	R14	Surface Mount Resistor 1206, 49.9 ohms
9	1	R15	Surface Mount Resistor 1206, 100 ohms
10	1	T1	Surface Mount Transformer Mini-Circuits T1–1T
11	1	U1	40.96 MHz Clock Oscillator
12	1	U2	AD9042AD 12-Bit–41 MSPS ADC Converter
13	2	U3, U4	74ACT574 Octal Latch
14	1	U5	74AS00 Quad Two Input NAND Gate

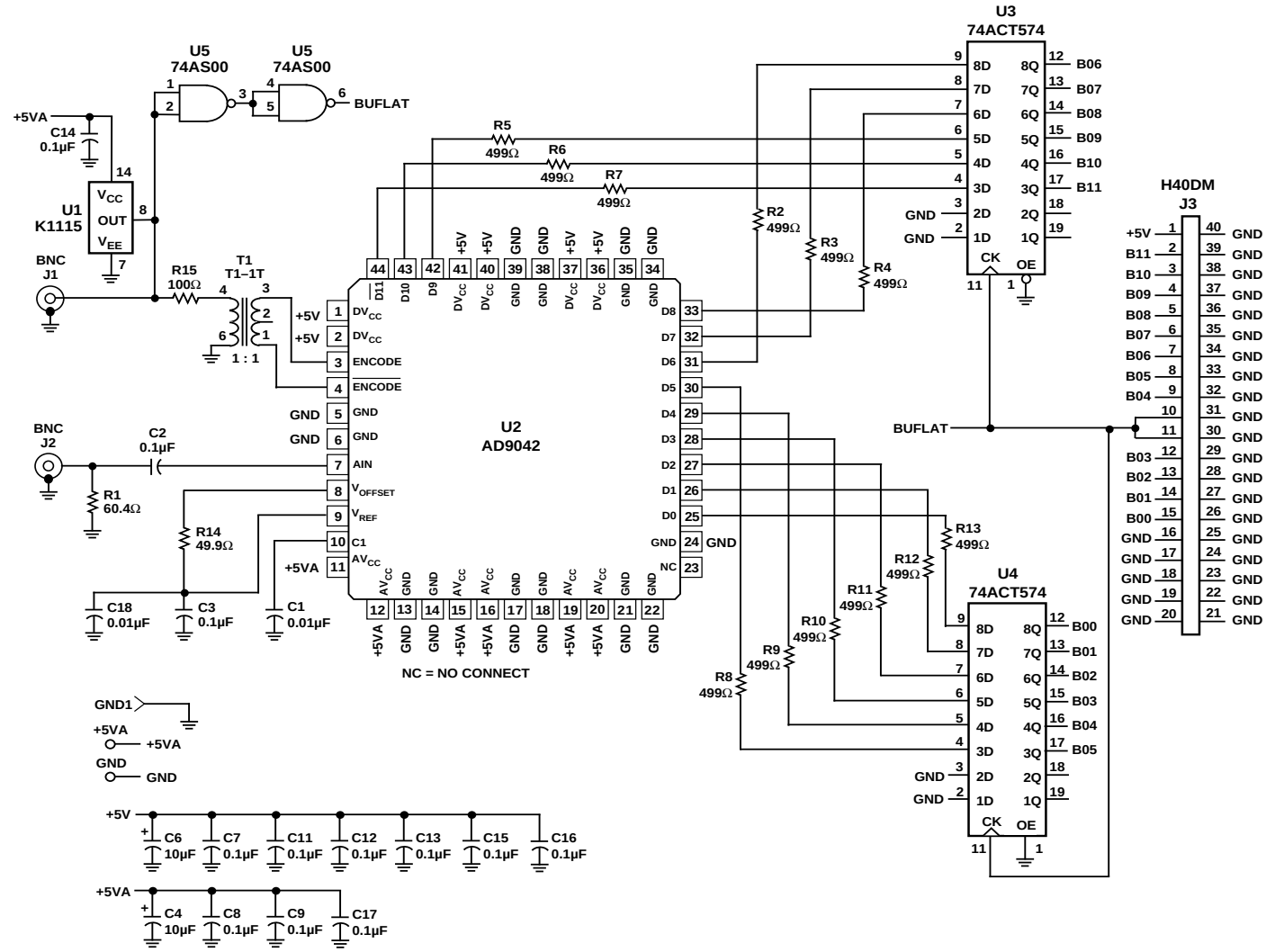


Figure 38. AD9042ST/PCB Schematic

Table II. AD9042ST/PCB Bill of Material

Item	Quantity	Reference	Description
1	2	+5VA, GND	Banana Jack
2	10	C2–C3, C7–C9, C11–C17	Ceramic Chip Capacitor 0805, 0.1 µF
3	2	C4, C6	Tantalum Chip Capacitor 10 µF
4	1	J3	40-Pin Double Row Male Header
5	2	J1, J2	BNC Coaxial PCB Connector
6	1	R1	Surface Mount Resistor 1206, 60.4 ohms
7	12	R2–R13	Surface Mount Resistor 1206, 499 ohms
8	1	R14	Surface Mount Resistor 1206, 49.9 ohms
9	1	R15	Surface Mount Resistor 1206, 100 ohms
10	1	T1	Surface Mount Transformer Mini-Circuits T1–1T
11	1	U1	40.96 MHz Clock Oscillator
12	1	U2	AD9042AST 12-Bit–41 MSPS ADC Converter
13	2	U3, U4	74ACT574 Octal Latch
14	1	U5	74AS00 Quad Two Input NAND Gate
15	1	C1, C18	Ceramic Chip Capacitor 0805, 0.01 µF AVX05085C103MA15

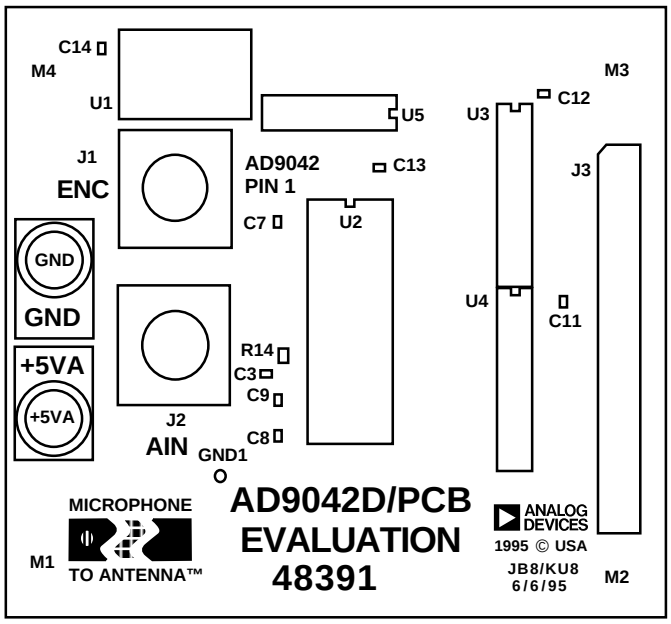


Figure 39. AD9042D/PCB Top Side Silk Screen

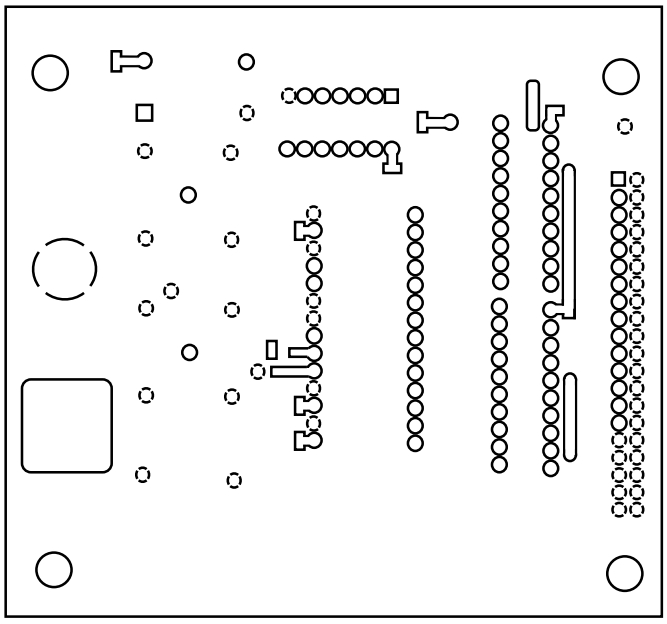


Figure 41. AD9042D/PCB Top Side Copper (Negative)

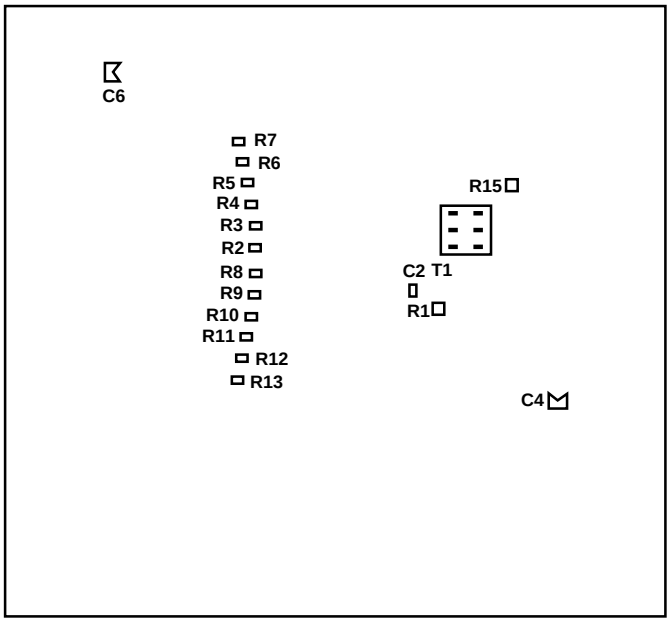


Figure 40. AD9042D/PCB Bottom Side Silk Screen

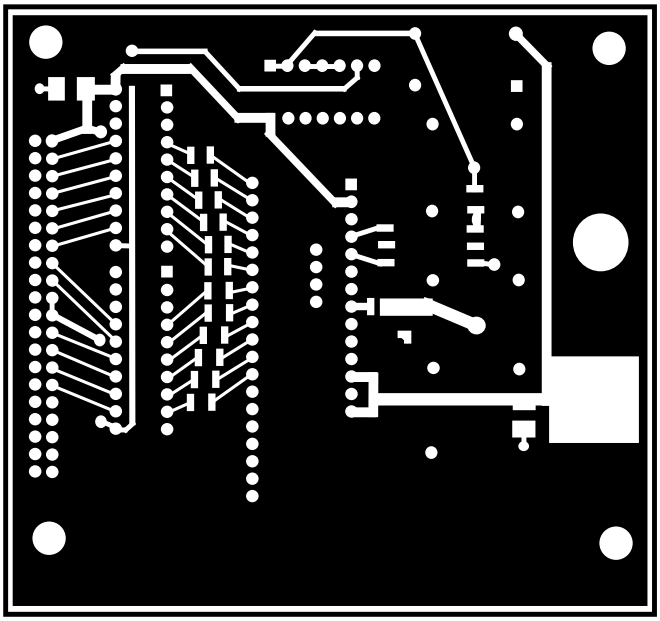


Figure 42. AD9042D/PCB Bottom Side Copper (Negative)

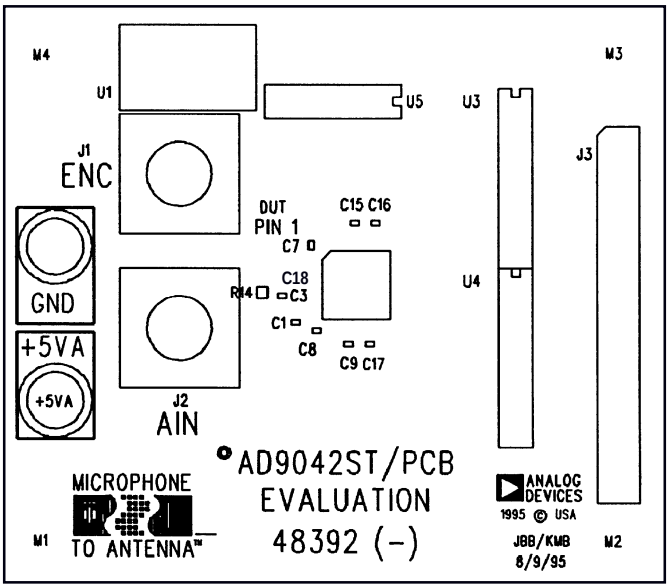


Figure 43. AD9042ST/PCB Top Side Silk Screen

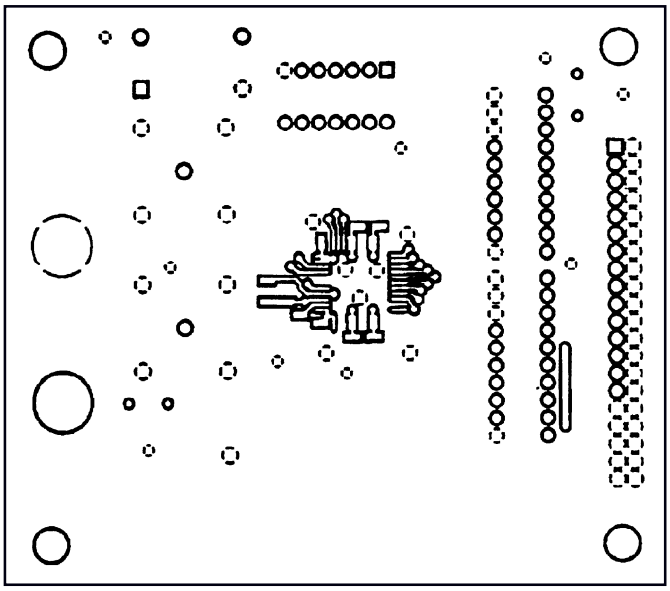


Figure 45. AD9042ST/PCB Top Side Copper (Negative)

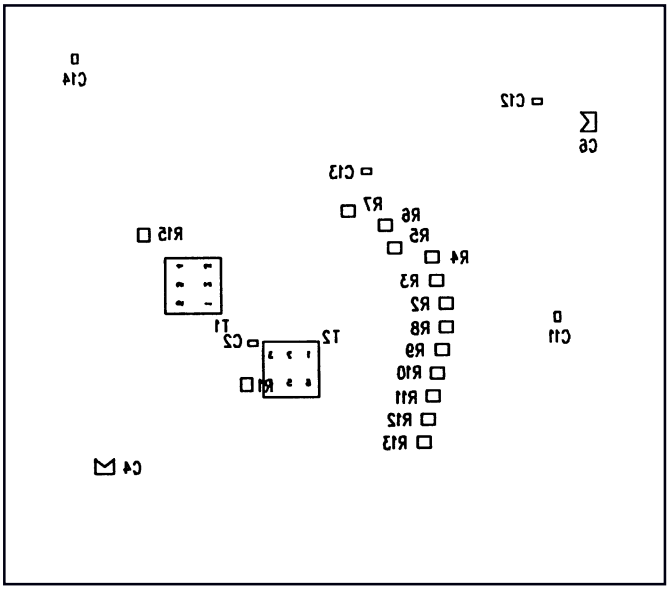


Figure 44. AD9042ST/PCB Bottom Side Silk Screen

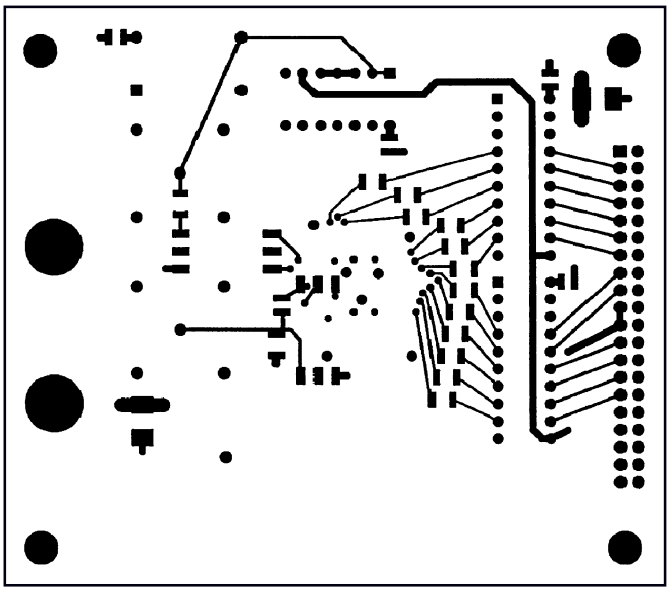


Figure 46. AD9042ST/PCB Bottom Side Copper (Positive)

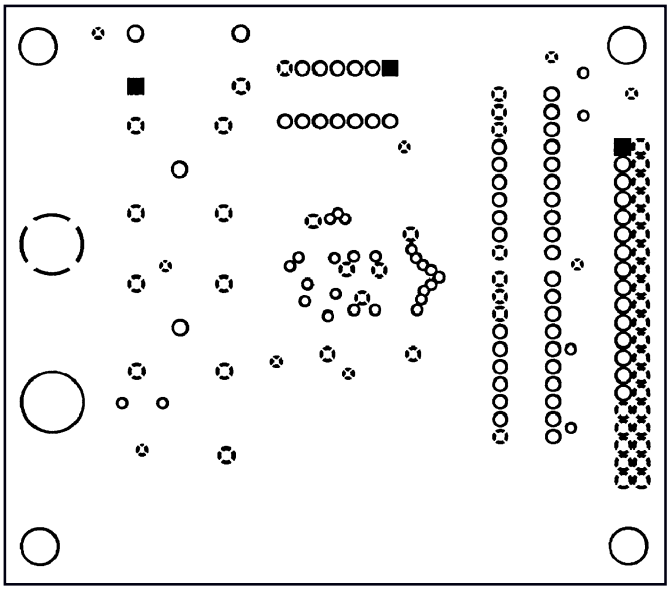


Figure 47. AD9042ST/PCB Grounded Layer (Negative)

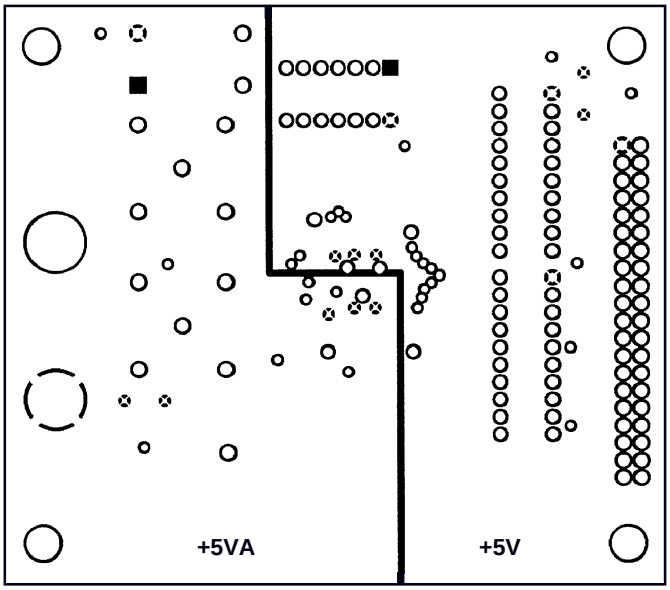


Figure 48. AD9042ST/PCB "Split" Power Layer (Negative)

DIGITAL WIDEBAND RECEIVERS

Introduction

Several key technologies are now being introduced that may forever alter the vision of radio. Figure 49 shows the typical dual conversion superheterodyne receiver. The signal picked up by the antenna is mixed down to an intermediate frequency (IF) using a mixer with a variable local oscillator (LO); the variable LO is used to "tune-in" the desired signal. This first IF is mixed down to a second IF using another mixer stage and a fixed LO. Demodulation takes place at the second or third IF using either analog or digital techniques.

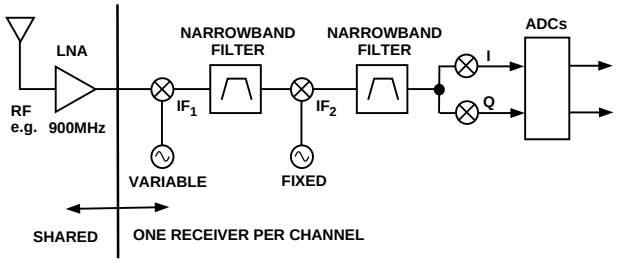


Figure 49. Narrowband Digital Receiver Architecture

If demodulation takes place in the analog domain then traditional discriminators, envelop detectors, phase locked loops or other synchronous detectors are generally employed to strip the modulation from the selected carrier.

However, as general purpose DSP chips such as the ADSP-2181 become more popular, they will be used in many baseband-sampled applications like the one shown in Figure 49. As shown in the figure, prior to ADC conversion, the signal must be mixed down, filtered, and the I and Q components separated. These functions are realizable through DSP techniques, however several key technology breakthroughs are required: high dynamic range ADCs such as the AD9042, new DSPs (highly programmable with onboard memory, fast), digital tuner & filter (with programmable frequency and BW) and wide band mixers (high dynamic range with >12.5 MHz BW).

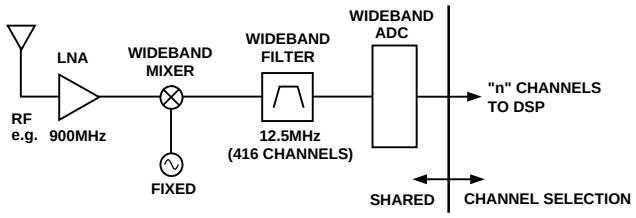


Figure 50. Wideband Digital Receiver Architecture

Figure 50 shows such a wideband system. This design shows that the front end variable local oscillator has been replaced with a fixed oscillator (for single band radios) and the back end has been replaced with a wide dynamic range ADC, digital tuner and DSP. This technique offers many benefits.

First, many passive discrete components have been eliminated that formed the tuning and filtering functions. These passive components often require "tweaking" and special handling during assembly and final system alignment. Digital components require no such adjustments; tuner and filter characteristics are always exactly the same. Moreover, the tuning and filtering characteristics can be changed through software. Since software is used for demodulation, different routines may be used to demodulate different standards such as AM, FM, GMSK or any other desired standard. In addition, as new standards arise or new software revisions are generated, they may be field installed with standard software update channels. A radio that performs demodulation in software as opposed to hardware is often referred to as a soft radio because it may be changed or modified simply through code revision.

System Description

In the wideband digital radio (Figure 50), the first down conversion functions in much the same way as a block converter does. An entire band is shifted in frequency to the desired intermediate frequency. In the case of cellular base station receivers, 5 MHz to 20 MHz of bandwidth are down-converted simultaneously to an IF frequency suitable for digitizing with a wideband analog-to-digital converter. Once digitized the broadband digital data stream contains all of the in-band signals. The remainder of the radio is constructed digitally using special purpose and general purpose programmable DSP to perform filtering, demodulation and signal conditioning not unlike the analog counter parts.

In the narrowband receiver (Figure 49), the signal to be received must be tuned. This is accomplished by using a variable local oscillator at the first mix down stage. The first IF then uses a narrow band filter to reject out of band signals and condition the selected carrier for signal demodulation.

In the digital wideband receiver (Figure 50), the variable local oscillator has been replaced with a fixed oscillator, so tuning must be accomplished in another manner. Tuning is performed digitally using a digital down conversion and filter chip frequently called a channelizer. The term channelizer is used because the purpose of these chips is to select one channel out of the many within the broadband of spectrum actually present in the digital data stream of the ADC.

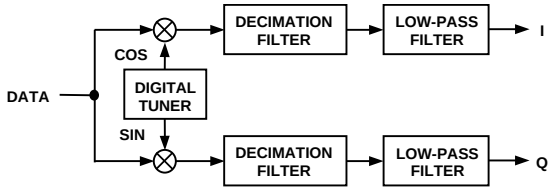


Figure 51. Digital Channelizer

Figure 51 shows the block diagram of a typical channelizer. Channelizers consist of a complex NCO (Numerically Controlled Oscillator), dual multiplier (mixer), and matched digital filters. These are the same functions that would be required in an analog receiver, however implemented in digital form. The digital output from the channelizer is the desired carrier, frequently in I & Q format; all other signals have been filtered and removed based on the filtering characteristics desired. Since the channelizer output consists of one selected RF channel, one tuner chip is required for each frequency received, although only one wideband RF receiver is needed for the entire band. Data from the channelizer may then be processed using a digital signal processor such as the ADSP-2181 or the SHARC processor, the ADSP-21062. This data may then be processed through software to demodulate the information from the carrier.

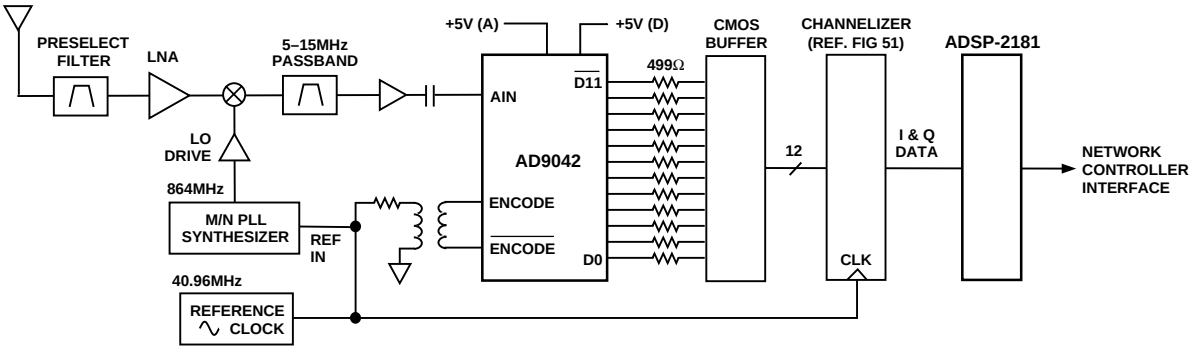


Figure 52. Simplified 5 MHz Wideband "A" Carrier Receiver

System Requirements

Figure 52 shows a typical wideband receiver subsystem based around the AD9042. This strip consists of a wideband IF filter, amplifier, ADC, latches, channelizer and interface to a digital signal processor. This design shows a typical clocking scheme used in many receiver designs. All timing within the system is referenced back to a single clock. While this is not necessary, it does facilitate PLL design, ease of manufacturing, system test, and calibration. Keeping in mind that the overall performance goal is to maintain the best possible dynamic range, many considerations must be made.

One of the biggest challenges is selecting the amplifier used to drive the AD9042. Since this is a communications application, the key specification for this amplifier is spurious-free dynamic range, or SFDR. An amplifier should be selected that can provide SFDR performance better than 80 dB into 250 ohms. One such amplifier is the AD9631. These low spurious levels are necessary as harmonics due to the drive amplifier and ADC could distort the desired signals of interest.

Two other key considerations for the digital wideband receiver are converter sample rate and IF frequency range. Since performance of the AD9042 converter is nearly independent of both sample rate and analog input frequency (Figures 11, 12, and 17), the designer has greater flexibility in the selection of these parameters. Also, since the AD9042 is a bipolar device, power dissipation is not a function of sample rate. Thus there is no penalty paid in power by operating at faster sample rates. All of this is good, because by carefully selecting input frequency range and sample rate, the drive amplifier and ADC harmonics can actually be placed out-of-band. Thus other components such as filters and IF amplifiers may actually end up being the limiting factor on dynamic range.

For example, if the system has second and third harmonics that are unacceptably high, by carefully selecting the encode rate and signal bandwidth, these second and third harmonics can be placed out-of-band. For the case of an encode rate equal to 40.96 MSPS and a signal bandwidth of 5.12 MHz, placing the fundamental at 5.12 MHz places the second and third harmonics out of band as shown in the table below.

Table III.

Encode Rate	40.96 MSPS
Fundamental	5.12 MHz–10.24 MHz
Second Harmonic	10.24 MHz–20.48 MHz
Third Harmonic	15.36 MHz–10.24 MHz

Another option can be found through bandpass sampling. If the analog input signal range is from dc to FS/2, then the amplifier and filter combination must perform to the specification required. However, if the signal is placed in the third Nyquist zone (FS to 3 FS/2), the amplifier is no longer required to meet the harmonic performance required by the system specifications since all harmonics would fall outside the passband filter. For example, the passband filter would range from FS to 3 FS/2. The second harmonic would span from 2 FS to 3 FS, well outside the passband filter's range. The burden then has been passed off to the filter design provided that the ADC meets the basic specifications at the frequency of interest. In many applications, this is a worthwhile tradeoff since many complex filters can easily be realized using SAW and LCR techniques alike at these relatively high IF frequencies. Although harmonic performance of the drive amplifier is relaxed by this technique, intermodulation performance cannot be sacrificed since intermods must be assumed to fall in-band for both amplifiers and converters.

Noise Floor and SNR

Oversampling is the act of sampling at a rate that is greater than twice the bandwidth of the signal desired. Oversampling does not have anything to do with the actual frequency of the sampled signal, it is the bandwidth of the signal that is key. Bandpass or "IF" sampling refers to sampling a frequency that is higher than Nyquist and often provides additional benefits such as down conversion using the ADC and track-and-hold as a mixer. Oversampling leads to processing gains because the faster the signal is digitized, the wider the distribution of noise. Since the integrated noise must remain constant, the actual noise floor is lowered by 3 dB each time the sample rate is doubled. The effective noise density for an ADC may be calculated by the equation:

$$V_{NOISE\ rms} / \sqrt{Hz} = \frac{10^{-SNR/20}}{\sqrt{4\ FS}}$$

For a typical SNR of 68 dB and a sample rate of 40.96 MSPS, this is equivalent to $31\ nV / \sqrt{Hz}$. This equation shows the relationship between SNR of the converter and the sample rate FS. This equation may be used for computational purposes to determine overall receiver noise.

The signal-to-noise ratio (SNR) for an ADC can be predicted. When normalized to ADC codes, the following equation accurately predicts the SNR based on three terms. These are jitter, average DNL error and thermal noise. Each of these terms contributes to the noise within the converter.

Equation 1:

$$SNR = -20\log\left[\left(2\pi F_{ANALOG}\ t_{J\,rms}\right)^2 + \left(\frac{1+\varepsilon}{2^{12}}\right)^2 + \left(\frac{V_{NOISE\,rms}}{2^{12}}\right)^2\right]^{1/2}$$

F_{ANALOG} = analog input frequency

$t_{J\,rms}$ = rms jitter of the encode (rms sum of encode source and internal encode circuitry)

ε = average DNL of the ADC

$V_{NOISE\,rms}$ = V rms thermal noise referred to the analog input of the ADC

Processing Gain

Processing gain is the improvement in signal-to-noise ratio (SNR) gained through DSP processes. Most of this processing gain is accomplished using the channelizer chips. These special purpose DSP chips not only provide channel selection and filtering but also provide a data rate reduction. Few, if any, general purpose DSPs can accept and process data at 40.96 MSPS. The required rate reduction is accomplished through a process called decimation. The term decimation rate is used to indicate the ratio of input data rate to output data rate. For example, if the input data rate is 40.96 MSPS and the output data rate is 30 kSPS, then the decimation rate is 1365.

Large processing gains may be achieved in the decimation and filtering process. The purpose of the channelizer, beyond tuning, is to provide the narrowband filtering and selectivity that traditionally has been provided by the ceramic or crystal filters of a narrowband receiver. This narrowband filtering is the source of the processing gain associated with a wideband receiver and is simply the ratio of the passband to whole band expressed in dB. For example, if a 30 kHz AMPS signal is being digitized with an AD9042 sampling at 40.96 MSPS, the ratio would be 0.030 *MHz*/20.48 *MHz*. Expressed in log form, the processing gain is $-10 \times \log$ (0.030 *MHz* / 20.48 *MHz*) or 28.3 dB!

Additional filtering and noise reduction techniques can be achieved through DSP techniques; many applications do use additional process gains through proprietary noise reduction algorithms.

Overcoming Static Nonlinearities with Dither

Typically, high resolution data converters use multistage techniques to achieve high bit resolution without large comparator arrays that would be required if traditional "flash" ADC techniques were employed. The multistage converter typically provides better wafer yields meaning lower cost and much lower power. However, since it is a multistage device, certain portions of the circuit are used repetitively as the analog input sweeps from one end of the converter range to the other. Although the worst DNL error may be less than an LSB, the repetitive nature of the transfer function can play havoc with low level dynamic signals. Spurious signals for a full-scale input may be –88 dBc, however 29 dB below full scale, these repetitive DNL errors may cause spurious-free dynamic range (SFDR) to fall to 80 dBc as shown in Figure 20.

A common technique for randomizing and reducing the effects of repetitive static linearity is through the use of dither. The purpose of dither is to force the repetitive nature of static linearity to appear as if it were random. Then, the average linearity over the range of dither will dominate SFDR performance. In the AD9042, the repetitive cycle is every 15.625 mV p-p.

To insure adequate randomization, 5.3 mV rms is required; this equates to a total dither power of –32.5 dBm. This will randomize the DNL errors over the complete range of the residue converter. Although lower levels of dither such as that from previous analog stages will reduce some of the linearity errors, the full effect will only be gained with this larger dither. Increasing dither even more may be used to reduce some of the global INL errors. However, signals much larger than the mVs proposed here begin to reduce the usable dynamic range of the converter.

Even with the 5.3 mV rms of noise suggested, SNR would be limited to 36 dB if injected as broadband noise. To avoid this problem, noise may be injected as an out-of-band signal. Typically, this may be around dc but may just as well be at FS/2 or at some other frequency not used by the receiver. The bandwidth of the noise is several hundred kilohertz. By band-limiting and controlling its location in frequency, large levels of dither may be introduced into the receiver without seriously disrupting receiver performance. The result can be a marked improvement in the SFDR of the data converter.

Figure 23 shows the same converter shown earlier but with this injection of dither (ref. Figure 20). Spurious-free dynamic range is now 94 dBFS. Figure 21 and 24 show an SFDR sweep before and after adding dither.

To more fully appreciate the improvement that dither can have on performance, Figures 22 and 25 show a before-and-after dither using additional data samples in the Fourier transform. Increasing to 128k sample points lowers the noise floor of the FFT; this simply makes it easier to "see" the dramatic reduction in spurious levels resulting from dither.

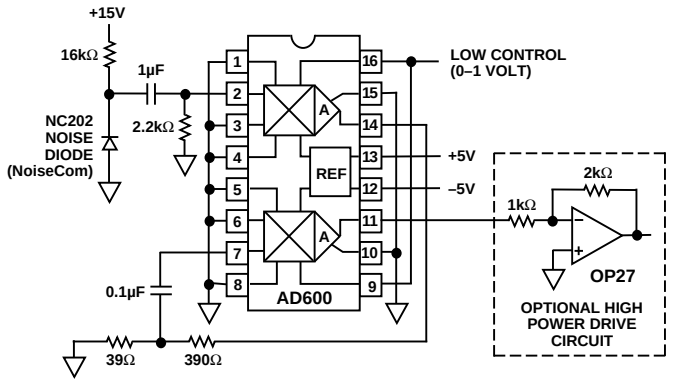


Figure 53. Noise Source (Dither Generator)

The simplest method for generating dither is through the use of a noise diode (Figure 53). In this circuit, the noise diode NC202 generates the reference noise that is gained up and driven by the AD600 and OP27 amplifier chain. The level of noise may be controlled by either presetting the control voltage when the system is set up, or by using a digital-to-analog converter (DAC) to adjust the noise level based on input signal conditions. Once generated, the signal must be introduced to the receiver strip. The easiest method is to inject the signal into the drive chain after the last down conversion as shown in Figure 54.

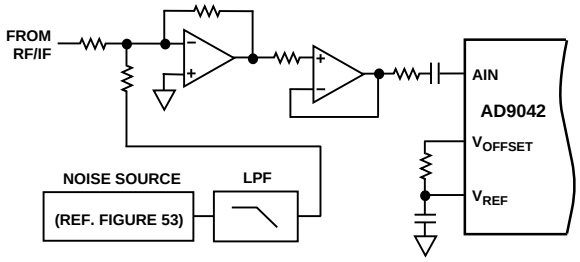


Figure 54. Using the AD9042 with Dither

Receiver Example

To determine how the ADC performance relates to overall receiver sensitivity, the simple receiver in Figure 55 will be examined. This example assumes that the overall down conversion process can be grouped into one set of specifications, instead of individually examining all components within the system and summing them together. Although a more detailed analysis should be employed in a real design, this model will provide a good approximation.

In examining a wideband digital receiver, several considerations must be applied. Although other specifications are important, receiver sensitivity determines the absolute limits of a radio excluding the effects of other outside influences. Assuming that receiver sensitivity is limited by noise and not adjacent signal strength, several sources of noise can be identified and their overall contribution to receiver sensitivity calculated.

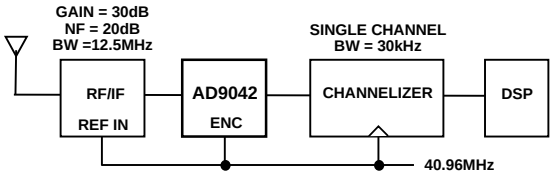


Figure 55. Receiver Analysis

The first noise calculation to make is based on the signal bandwidth at the antenna. In a typical broadband cellular receiver, the IF bandwidth is 12.5 MHz. Given that the power of noise in a given bandwidth is defined by $P_n = kTB$, where B is bandwidth, $k = 1.38 \times 10^{-23}$ is Boltzman's constant and $T = 300k$ is absolute temperature, this gives an input noise power of 5.18×10^{-14} watts or –102.86 dBm. If our receiver front end has a gain of 30 dB and a noise figure of 20 dB, then the total noise presented to the ADC input becomes –52.86 dBm (–102.86 + 30 + 20) or 0.51 mV rms. Comparing receiver noise to dither required for good SFDR, we see that in this example, our receiver supplies about 10% of the dither required for good SFDR.

Based on a typical ADC SNR specification of 68 dB, the equivalent internal converter noise is 0.140 mV rms. Therefore total broadband noise is 0.529 mV rms. Before processing gain, this is an equivalent SNR (with respect to full scale) of 56.5 dB. Assuming a 30 kHz AMPS signal and a sample rate of 40.96 MSPS, the SNR through processing gain is increased by 28.3 dB to 84.8 dB. However, if 8 strong and equal signals are present in the ADC bandwidth, then each must be placed 18 dB below full scale to prevent ADC overdrive. In addition, 3 dB to 15 dB should be used for ADC headroom should another signal come in-band unexpectedly. For this example, 12 dB of headroom will be allocated. Therefore we give away 30 dB of range and reduce the carrier-to-noise ratio (C/N)* to 54.8 dB.

Assuming that the C/N ratio must be 6 dB or better for accurate demodulation, one of the eight signals may be reduced by 48.8 dB before demodulation becomes unreliable. At this point, the input signal power would be 40.6 μV rms on the ADC input or –74.8 dBm. Referenced to the antenna, this is –104.8 dBm.

To improve sensitivity, several things can be done. First, the noise figure of the receiver can be reduced. Since front end noise dominates the 0.529 mV rms, each dB reduction in noise figure translates to an additional dB of sensitivity. Second, providing broadband AGC can improve sensitivity by the range of the AGC. However, the AGC would only provide useful improvements if all in-band signals are kept to an absolute minimal power level so that AGC can be kept near the maximum gain.

This noise limited example does not adequately demonstrate the true limitations in a wideband receiver. Other limitations such as SFDR are more restrictive than SNR and noise. Assume that the analog-to-digital converter has an SFDR specification of –80 dBFS or –76 dBm (Full scale = +4 dBm). Also assume that a tolerable carrier-to-interferer (C/I)** (different from C/N) ratio is 18 dB. This means that the minimum signal level is –62 dBFS (–80 plus 18) or –58 dBm. At the antenna, this is –88 dBm. Therefore, as can be seen, SFDR (single or multitone) would limit receiver performance in this example. However, as shown previously, SFDR can be greatly improved through the use of dither (Figures 22, 25). In many cases, the addition of the out-of-band dither can improve receiver sensitivity nearly to that limited by thermal noise.

Multitone Performance

The plot below shows the AD9042 in a worst case scenario of four strong tones spaced fairly close together. In this plot no dither was used, and the converter still maintained 85 dBFS of spurious-free range. As illustrated previously, a modest amount of dither introduced out-of-band could be used to lower the nonlinear components.

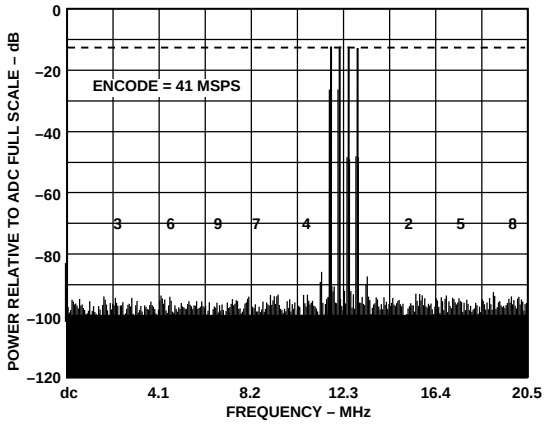


Figure 56. Multitone Performance

*C/N is the ratio of signal to inband noise.
**C/I is the ratio of signal to inband interferer.

IF Sampling, Using the AD9042 as a Mix-Down Stage

Since performance of the AD9042 extends beyond the baseband region into the second and third Nyquist zone, the converter may find many uses as a mix down converter in both narrowband and wideband applications. Many common IF frequencies exist in this range of frequencies. If the ADC is used to sample these signals, they will be aliased down to baseband during the sampling process in much the same manner that a mixer will down-convert a signal. For signals in various Nyquist zones, the following equation may be used to determine the final frequency after aliasing.

$$f_{1NYQUISTS} = f_{SAMPLE} - f_{SIGNAL}$$
$$f_{2NYQUISTS} = abs\,(f_{SAMPLE} - f_{SIGNAL})$$
$$f_{3NYQUISTS} = 2 \times f_{SAMPLE} - f_{SIGNAL}$$
$$f_{4NYQUISTS} = abs\,(2 \times f_{SAMPLE} - f_{SIGNAL})$$

Using the converter to alias down these narrowband or wideband signals has many potential benefits. First and foremost is the elimination of a complete mixer stage, along with amplifiers, filters and other devices, reducing cost and power dissipation.

One common example is the digitization of a 21.4 MHz IF using a 10 MSPS sample clock. Using the equation above for the fifth Nyquist zone, the resultant frequency after sampling is 1.4 MHz. Figure 57 shows performance under these conditions. Even under these conditions, the AD9042 typically maintains better than 80 dB SFDR.

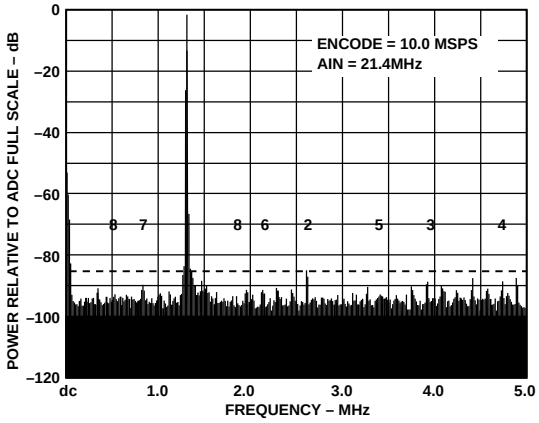


Figure 57. IF-Sampling a 21.4 MHz Input

RECEIVE CHAIN FOR DIGITAL BEAM-FORMING MEDICAL ULTRASOUND USING THE AD9042

The AD9042 is an excellent digitizer for digital and analog beam-forming medical ultrasound systems. The price/ performance ratio of the AD9042 allows ultrasound designers the luxury of using state-of-the-art ADCs without jeopardizing their cost budgets. ADC performance is critical for image quality. The high dynamic range and excellent noise performance of the AD9042 enable higher image quality medical ultrasound systems.

Figure 58 shows the AD9042 used in one channel of the receive chain of a medical ultrasound system. The AD604 receives its input directly from the transducer, or from an external preamp connected to the transducer. The AD604 contains two separate stages. The first stage is a preamp with a fixed gain (14 dB to 20 dB) selected by a fixed resistor. The second stage is a variable gain amplifier with the gain set by the AD7226 DAC. The gain is increased over time to compensate for the attenuation of signal level in the body.

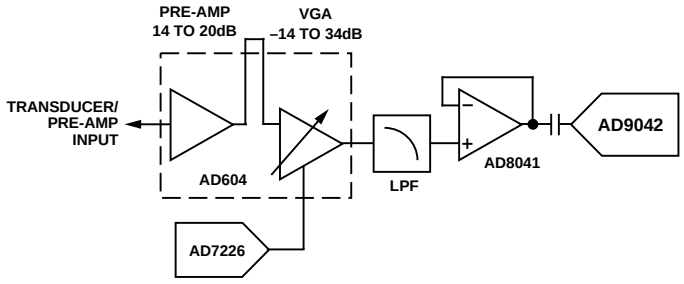


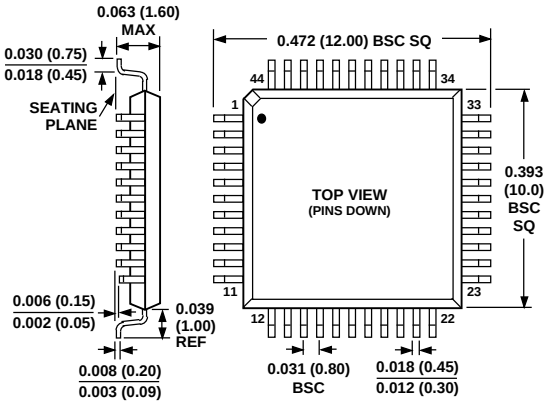
Figure 58. Using the AD9042 in Ultrasound Applications

Following the AD604, a low-pass filter is used to minimize the amount of noise presented to the ADC. The AD8041 is used to buffer the filter from the AD9042 input. This function may not be required depending on the filter configuration and PC board partitioning. The digital outputs of the AD9042 are then presented to the digital system for processing.

AD9042AST OUTLINE DIMENSIONS

Dimensions shown in inches and (mm)

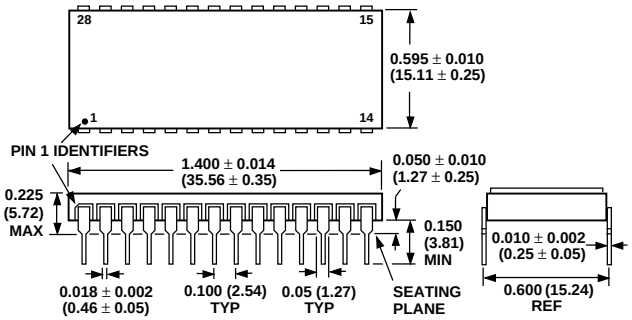
44-Pin Thin Quad Flatpack (ST-44)



AD9042AD OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Pin Hermetic Ceramic DIP (DH-28)



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